AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)

(Approved by AICTE | Accredited by NAAC | Affiliated to JNTUA)

Gudur, Nellore Dist - 524101, A.P (India)

OUTCOME BASED EDUCATION

WITH

CHOICE BASED CREDIT SYSTEM

MASTER OF TECHNOLOGY

VLSI

ACADEMIC REGULATIONS

UNDER AUTONOMOUS STATUS

M.Tech Regular Two Year PG Programme

(for the batches admitted from the academic year 2018 - 2019)

ACADEMIC REGULATIONS (R18) FOR M.TECH. REGULAR STUDENTS WITH EFFECT FROM ACADEMIC YEAR 2018-2019

1.0 Post- Graduate Degree Programme in Engineering & Technology

1.1 These academic rules and regulations are applicable to the students admitted from the academic year 2018-19 onwards into 2 year (4 Semesters) M.Tech Programmes under Choice Based Credit System(CBCS) at its autonomous institution with effect from the academic year 2018-19 in the following specializations of Engineering:

M.Tech Specializations offered

1. Embedded Systems (ES)
2. VLSI (VL)
3. Electrical Power Systems (EP)
4. Power Electronics (PE)
5. Computer Science & Engineering (CO)
6. Software Engineering (SE)
7. Structural Engineering (ST)

2.0	**Eligibility for admission**
2.1	Admission to the post graduate programme shall be made either on the basis of the merit rank obtained by the qualified student in entrance test PGECET conducted by the Andhra Pradesh State Government as per the norms of Andhra Pradesh State Council of Higher Education (APSCHE)
2.2	The medium of instructions for the entire post graduate programme in Engineering & Technology will be English only.
3.0	**M.Tech. Programme Pattern**
3.1	A student after securing admission shall pursue the post graduate programme in M.Tech in a minimum period of two academic years (4 semesters), and a maximum period of four academic years (8 semesters) starting from the date of commencement of first year first semester, failing which student shall forfeit the M.Tech course. Each semester is structured to around 20 credits, totaling to 78 credits for the entire M.Tech programme. Each student shall secure 78 credits required for the completion of the post graduate programme and award of the M.Tech degree.
3.2	A student eligible to appear for the end examination in a course, but absent or has failed in the end examination may appear for that course at the next supplementary examination when offered
3.3	When a student is detained due to lack of shortage of attendance he/she may be re-admitted when the semester is offered after fulfillment of academic regulations. In such case, he/she shall be in the academic regulations into which he/she is readmitted.

3.4	UGC/ AICTE specified definitions/ descriptions are adopted appropriately for various terms and abbreviations used in these academic regulations/ norms, which are listed below.
3.5	**Semester scheme** Each under graduate programme is of 2 academic years (4 semesters) with the academic year being divided into two semesters of 16 weeks (around 90 instructional days) each and semester having – Continuous Internal Evaluation (CIE) and Semester End Examination (SEE). Choice based Credit System (CBCS) and Credit Based Semester System (CBSS) as indicated by UGC and curriculum / course structure as suggested by AICTE are followed.
3.6	**Credit courses** All subjects/ courses are to be registered by the student in a semester to earn credits which shall be assigned to each subject/ course in an L: T: P: C (lecture periods: Tutorial periods: Practical periods: Credits) structure based on the following general pattern. • One credit for one hour/ week/ semester for theory/ lecture (L) courses. • One credit for two hours/ week/ semester for laboratory/ practical (P) courses or Tutorials (T).
3.7	**Subject Course Classification** All subjects/ courses offered for the post graduate programme in Engineering & Technology (M.Tech. degree programmes) are broadly classified as follows. The ASCET has followed almost all the guidelines issued by AICTE/UGC.
4.0	**Attendance requirements:**
4.1	A student shall be eligible to appear for the semester end examinations, if student acquires a minimum of 75% of attendance in aggregate of all the subjects/ courses for that semester.
4.2	Shortage of attendance in aggregate up to 10% (65% and above, and below 75%) in each semester may be condoned by the college academic committee on genuine and valid grounds, based on the student's representation with supporting evidence.
4.3	A stipulated fee shall be payable towards condonation for shortage of attendance to the institute as decided by the College Academic Committee.
4.4	Shortage of attendance below 65% in aggregate shall in no case be condoned.
4.5	Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examinations of that semester. They get detained and their registration for that semester shall stand cancelled. They will not be promoted to the next semester. They may seek re-registration for all those subjects registered in that semester in which student was detained, by seeking re-admission into that semester as and when offered; in case if there are any professional electives and/ or open electives, the same may also be re-registered if offered. However, if those electives are not offered in later semesters, then alternate electives may be chosen from the same set of elective subjects offered under that category.
4.6	A student fulfilling the attendance requirement in the present semester shall not be eligible for readmission into the same class.
5.0	**Academic requirements** The following academic requirements have to be satisfied, in addition to the attendance requirements mentioned in item no.4.

5.1	A student shall be deemed to have satisfied the minimum academic requirements and earned the credits allotted to each theory, practical, design, drawing subject or project if he secures not less than 40% of marks (i.e., 24) in the end semester examination and a minimum of 50% of marks (i.e., 50) in the sum total of the internal evaluation and end examination taken together.
5.6	A student shall register and put up minimum attendance in all 78 credits and earn all the 78 credits. Marks obtained in all 78 credits shall be considered for the calculation of aggregate percentage of marks obtained
5.7	Students who fail to earn 78 credits as indicated in the course structure within eight academic years from the year of their admission shall forfeit their seat in M.Tech. Course and their admission shall stand cancelled
6.0	**Distribution and Weightage of marks**
6.1	The performance of a student in each semester shall be evaluated through internal evaluation and /or an external evaluation conducted semester wise.
6.2	The performance of a student in every theory course shall be evaluated for total of 100 marks each, of which the relative weightage for Continuous Internal Evaluation and Semester End Examination shall be 40 marks and 60 marks respectively.
6.3	The performance of a student in every practical course shall be evaluated for total of 75 marks each, of which the relative weightage for Continuous Internal Evaluation and Semester End Examination shall be 25 marks and 50 marks respectively.
6.4	**Internal Evaluation for Theory Course:** The total internal weightage for theory courses is 40 marks with the following distribution. ➢ 30 marks for Mid-Term Examination ➢ 10 marks for Assignment Test While the first mid-term examination shall be conducted on the 50% of the syllabus (Unit-I, Unit-II, & 50% of Unit-III), the second mid-term examination shall be conducted on the remaining 50% of the syllabus (50 % of Unit III, Unit-IV & Unit-V). 10 marks are allocated for assignment test (as specified by the subject teacher concerned). The first assignment should be conducted after completion of Unit-I for 5 marks and the second assignment should be conducted after completion of Unit- IV for 5 marks. The final Assignment Test marks will be the addition of these two. Two midterm examinations each for **30 marks** with the duration of 90 minutes each will be conducted for every theory course in a semester. The midterm examination marks shall be awarded giving a weightage of 80% in the midterm examination in which the student scores better performance and 20% in the remaining midterm examination. The final mid-term marks obtain by the addition of these two (80% + 20%). **Example**: If a student scores 33 marks and 34 marks in the first and second mid-term examinations respectively, then Weighted Average Marks = 34 x 0.8 + 33 x 0.2 = 33.8, rounded to 34 Marks. **Note**: The marks of any fraction shall be rounded off to the next higher mark.
6.5	**Pattern of the midterm examination question paper is as follows:** ➢ A total of three questions ➢ Question paper contains six questions are to be designed taking three questions from

	each unit (Unit Wise - Either or type) of the three units. (3X10=30 Marks) **Pattern of the Assignment Test is as follows:** ➢ Five assignment questions are given in advance, out of which two questions given by the concerned teacher has to be answered during the assignment test ➢ Sum of Assignment Tests marks is considered. **Note:** A student who is absent for any Mid-Term Examination/ Assignment Test, for any reason whatsoever, shall be deemed to have scored zero marks in that Mid-Term Examination/ Assignment Test and no make-up test shall be conducted.
6.6	**Internal Evaluation for Practical Course:** For practical subjects there shall be a Continuous Internal Evaluation during the semester for 25 internal marks. Out of the 25 marks for internal evaluation, day-today assessment in the laboratory shall be evaluated for 10 marks and internal practical examination shall be evaluated for 15 marks conducted by the laboratory teacher concerned.
6.7	**Internal Evaluation for Term Paper:** The Term Paper is a self study report and shall be carried out either during II semester along with other lab courses. Every student will take up this term paper individually and submit a report. The scope of the term paper could be an exhaustive literature review choosing any engineering concept with reference to standard research papers or an extension of the concept of earlier course work in consultation with the term paper supervisor. The term paper reports submitted by the individual students during the II semester shall be evaluated for a total of 50 marks for continuous assessment; it shall be conducted by two Examiners, one of them being term paper supervisor as internal examiner and an external examiner nominated by the Principal from the panel of experts recommended by HOD.
6.8	**Project Work:** The Project work is spread over to two semesters having Project Work Phase-I and Project Work Phase-II. Project Work Phase-I is included in III Semester and Project Work Phase-II in IV Semester as detailed below: A student has to select topic of his Project Work based on his interest and available facilities, in the III semester which he will continue through IV semester also.
6.9	**External Evaluation for Theory Course - Semester End Examination:** The Semester End Examination in each theory subject shall be conducted for 3 hours duration at the end of the semester for 60 marks. **Pattern of the Semester End Examination question paper is as follows:** ➢ Question Paper contains ten questions are to be designed taking two questions from each unit (Unit Wise - Either or type) of the total five units. (5X12=60 Marks) A student has to secure not less than a minimum of 40% of marks (24 marks) exclusively at the Semester End Examinations in each of the theory subjects in which the candidate had appeared. However, the candidate shall have to secure a minimum of 50% of marks (50 marks) in both external and internal components put together to become eligible for passing in the subject.
6.10	**External Evaluation for Practical Course** Out of 50 marks **35** marks are allocated for experiment (procedure for conducting the experiment carries 15 marks & readings, calculation and result-20) and **10** marks for viva-

voce examination with **5** marks for the record.

Each Semester External Lab Examination shall be evaluated by an Internal Examiner along with an External Examiner appointed by the Principal.

A candidate shall be declared to have passed in individual lab course if he secures a minimum of 50% aggregate marks (38 marks) (Internal & Semester External Examination marks put together), subject to a minimum of 50% marks (25 marks) in the semester external examination.

6.11 Project Work Phase-I:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ concerned department.

- **Registration of Project work**: A candidate is permitted to register for the project work phase-I after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Semesters).
- An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor/ Guide and one Internal senior expert shall monitor the progress of the project work.
- The work on the project work phase-I shall be initiated in the III semester and continued in the final semester. The candidate can submit Project work phase-I dissertation with the approval of I.D.C. after 18 weeks from the date of registration at the earliest from the date of registration for the project work phase-I.
- The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.
- Three copies of the Dissertation certified in the prescribed form by the supervisor and HOD shall be submitted to the HOD.
- The semester end examination for project work phase-I done during III Semester, shall be conducted by a Project Review Committee (PRC). The evaluation of project work shall be conducted at the end of the III Semester.
- The PRC comprises of an External examiner appointed by the Principal, Head of the Department and Project Guide/Supervisor to adjudicate the dissertation. The PRC shall jointly evaluate candidates work and award grades as given below.

S.No	Description	Grade	Grade Point (GP) Assigned
1	Very Good	Grade A	10
2	Good	Grade B	9
3	Satisfactory	Grade C	8
4	Not satisfactory	Grade D	0

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the dissertation.

6.12 Project Work Phase-II:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ concerned department.

- **Registration of Project work**: A candidate is permitted to register for the project work phase-I after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Semesters)
- An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor/ Guide and one Internal senior expert shall monitor the progress of the project work.
- The work on the project work phase-II shall be initiated in the IV semester. The candidate can submit Project work phase-II dissertation with the approval of I.D.C. after 18 weeks from the date of registration at the earliest from the date of registration for the project work phase-I.
- The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.
- Three copies of the Dissertation certified in the prescribed form by the supervisor and HOD shall be submitted to the HOD.
- The semester end examination for project work phase-I done during III Semester, shall be conducted by a Project Review Committee (PRC). The evaluation of project work shall be conducted at the end of the IV Semester.
- The PRC comprises of an External examiner appointed by the Principal, Head of the Department and Project Guide/Supervisor to adjudicate the dissertation. The PRC shall jointly evaluate candidates work and award grades as given below

S.No	Description	Grade	Grade Point (GP) Assigned
1	Very Good	Grade A	10
2	Good	Grade B	9
3	Satisfactory	Grade C	8
4	Not satisfactory	Grade D	0

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the dissertation.

6.13 <u>Re-Registration For Improvement of Internal Evaluation Marks:</u>

Following are the conditions to avail the benefit of improvement of internal evaluation marks.

- The candidate should have completed the course work and obtained examinations results for I, II & III semesters.
- He should have passed all the subjects for which the internal evaluation marks secured are more than 50%.
- Out of the subjects the candidate has failed in the examination due to Internal evaluation marks secured being less than 50%, the candidate shall be given one more chance for each Theory subject and for a maximum of **<u>three</u>** Theory subjects for Improvement of

Internal evaluation marks.

- ❖ The candidate has to re-register for the subjects so chosen and fulfill all the academic requirements.
- ❖ For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of **'The Principal, Audisankara College of Engineering & Technology' payable at Gudur** along with the requisition through the Controller of the Examinations of the college.
- ❖ In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

7.0 **SEMESTER – WISE DISTRIBUTION OF CREDITS**

Semester	Theory	Practicals	Credits
M.Tech I Semester	5	2	22
M.Tech II Semester	4	2 + Term Paper	22
M.Tech III Semester	2	Project Work Phase-I	18
M.Tech IV Semester	0	Project Work Phase-II	16
		Total	78

8.0 **GRADING PROCEDURE**

Grades will be awarded to indicate the performance of students in each theory subject, laboratory / practicals, Term Paper and project Work Phase-I & II. Based on the percentage of marks obtained (Continuous Internal Evaluation plus Semester End Examination, both taken together) as specified in item 6 above, a corresponding letter grade shall be given.

8.1 As a measure of the performance of a student, a 10-point absolute grading system using the following letter grades (as per UGC/AICTE guidelines) and corresponding percentage of marks shall be followed:

Marks Range	Letter Grade	Grade Points
91-100	S (Superior)	10
81-90	A (Excellent)	9
70-80	B (Very Good)	8
60-69	C (Good)	7
55-59	D (Average)	6
50-54	E (Pass)	5
<50	F (FAIL)	0
Ab (Absent)	Ab	0

8.2	A student who has obtained an 'F' grade in any subject shall be deemed to have 'failed' and is required to reappear as a 'supplementary student' in the semester end examination, as and when offered. In such cases, internal marks in those subjects will remain the same as those obtained earlier
8.3	To a student who has not appeared for an examination in any subject, 'Ab' grade will be allocated in that subject, and he is deemed to have 'failed'. A student will be required to reappear as a 'supplementary student' in the semester end examination, as and when offered next. In this case also, the internal marks in those subjects will remain the same as those obtained earlier.
8.4	A letter grade does not indicate any specific percentage of marks secured by the student, but it indicates only the range of percentage of marks.
8.5	A student earns grade point (GP) in each subject/ course, on the basis of the letter grade secured in that subject/ course. The corresponding 'credit points' (CP) are computed by multiplying the grade point with credits for that particular subject/ course. Credit points (CP) = grade point (GP) x credits …. For a course
8.6	A student passes the subject/ course only when GP ≥5 ('E' grade or above)
8.7	➢ A student obtaining Grade F shall be considered failed and will be required to reappear for that subject when the next supplementary examination offered. ➢ For Mandatory courses "Satisfactory" or "Unsatisfactory" shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA.
8.8	**Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):** The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e. $$SGPA = \sum_{i=1}^{n}(Ci \times Gi) / \sum_{i=1}^{n} Ci$$ Where, Ci is the number of credits of the i^{th} subject, Gi is the grade point scored by the student in the i^{th} course and n is the number of subjects. The Cumulative Grade Point Average (CGPA) will be computed in the same manner taking into account all the courses undergone by a student over all the semesters of a program, i.e. $$CGPA = \sum_{i=1}^{n}(Ci \times Si) / \sum_{i=1}^{n} Ci$$ Where 'Si' is the SGPA of the i^{th} semester, Ci is the total number of credits in that semester and n is the number of semesters. Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts. While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included. ***Grade Point:*** It is a numerical weight allotted to each letter grade on a 10-point scale.

	Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by letters as mentioned in the above table.
9.0	**Award of Class**
9.1	After a student has satisfied the requirement prescribed for the completion of the program and is eligible for the award of M.Tech. Degree he/she shall be placed in one of the following four classes:

Class Awarded	CGPA Secured
First class with Distinction	>= 8
First class	>= 7 and < 8
Second class	>= 5 and < 7

10.0	**Transitory regulations**
10.1	For students detained due to shortage of attendance: 1. A Student who has been detained in I year of R16 Regulations due to lack of attendance, shall be permitted to join I year I Semester of R18 Regulations and he is required to complete the study of M.Tech/ programme with in the stipulated period of eight academic years from the date of first admission in I year. 2. A student who has been detained in any semester of II, III and IV years of R16 regulations for want of attendance, shall be permitted to join the corresponding semester of R18 regulations and is required to complete the study of M.Tech within the stipulated period of eight academic years from the date of first admission in I Year. The R18 Academic Regulations under which a student has been readmitted shall be see rule 10.3 for further Transitory Regulations.
10.2	For students detained due to shortage of credits: A student of R16 Regulations who has been detained due to lack of credits, shall be promoted to the next semester of R18 Regulations only after acquiring the required credits as per the corresponding regulations of his/her first admission. The student is required to complete the study of M.Tech. within the stipulated period of eight academic years from the year of first admission. The R18 Academic Regulations are applicable to a student from the year of readmission onwards. See rule 10.3 for further Transitory Regulations.
10.3	For readmitted students in R18 Regulations: 1. A student who has failed in any subject under any regulation has to pass those subjects in the same regulations. 2. The maximum credits that a student acquires for the award of degree, shall be the sum of the total number of credits secured in all the regulations of his/her study including R18 Regulations. 3. If a student readmitted to R18 Regulations, has any subject with 80% of syllabus common with his/her previous regulations, that particular subject in R18 Regulations will be substituted by another subject to be suggested by the College standing committee.

	Note: If a student readmitted to R18 Regulations, has not studied any subjects/topics in his/her earlier regulations of study which is prerequisite for further subjects in R18 Regulations, the department HOD concerned shall conduct remedial classes to cover those subjects/topics for the benefit of the students.
11.0	**Supplementary Examinations:** Apart from the regular End Examinations the institute may also schedule and conduct supplementary examinations for all subjects for the benefit of students with backlogs. Such students writing supplementary examinations as supplementary candidates may have to write more than one examination per day.
12.0	**Student Transfers** Student transfers shall be as per the guidelines issued by the Government of Andhra Pradesh from time to time.
13.0	**With–Holding of Results** If the candidate has any dues not paid to the institute or if any case of indiscipline or malpractice is pending against him/her, the result of the candidate shall be withheld and he/she will not be allowed / promoted into the next higher semester. The issue of awarding degree is liable to be withheld in such cases.
12.0	**Conduct and Discipline** ➢ Students shall conduct themselves within and outside the premises of the Institute in a descent and dignified manner befitting the students of Audisankara College of Engineering & Technology. ➢ As per the order of the Honorable Supreme Court of India, ragging in any form is considered a criminal offence and is totally banned. Any form of ragging will be severely dealt with The following acts of omission and / or commission shall constitute gross violation of the code of conduct and are liable to invoke disciplinary measures with regard to ragging. (i) Lack of courtesy and decorum; indecent behavior anywhere within or outside the college campus. (ii) Damage of college property or distribution of alcoholic drinks or any kind of narcotics to fellow students / citizens. ➢ Possession, consumption or distribution of alcoholic drinks or any kind of narcotics or hallucinogenic drugs. ➢ Mutilation or unauthorized possession of library books. ➢ Noisy and unruly behavior, disturbing studies of fellow students. ➢ Hacking in computer systems (such as entering into other person's areas without prior permission, manipulation and / or damage of computer hardware and software or any other cyber crime etc. ➢ Usage of camera /cell phones in the campus. ➢ Plagiarism of any nature. ➢ Any other act of gross indiscipline as decided by the college academic council from

	time to time. ➢ Commensurate with the gravity of offense, the punishment may be reprimand, fine, expulsion from the institute/ hostel, debarring from examination, disallowing the use of certain facilities of the Institute, rustication for a specified period or even outright expulsion from the Institute, or even handing over the case to appropriate law enforcement authorities or the judiciary, as required by the circumstances. ➢ For an offence committed in (i) a hostel (ii) a department or in a class room and (iii) elsewhere, the chief Warden, the concern Head of the Department and the Principal respectively, shall have the authority to reprimand or impose fine. ➢ Cases of adoption of unfair means and/ or any malpractice in an examination shall be reported to the principal for taking appropriate corrective action. ➢ All cases of serious offence, possibly requiring punishment other than reprimand, shall be reported to the Academic council of the college. ➢ The Institute Level Standing Disciplinary Action Committee constituted by the academic council shall be the authority to investigate the details of the offence, and recommend disciplinary action based on the nature and extent of the offence committed. ➢ The Principal shall deal with any problem, which is not covered under these rules and regulations. ➢ **"Grievance and Redressal Committee" (General)** constituted by the Principal shall deal with all grievances pertaining to the academic / administrative / disciplinary matters. ➢ All the students must abide by the code and conduct rules prescribed by the college from time to time.
13.0	**General** ➢ s/he represents "she" and "he" both ➢ Where the words 'he', 'him', 'his', occur, they imply 'she', 'her', 'hers' also. ➢ The academic regulations should be read as a whole for the purpose of any interpretation. ➢ In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman, Academic Council will be final. The college may change or amend the academic regulations or syllabi from time to time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the institute.

RULES FOR
DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers, blue tooth or any other form of material concerned with or related to the course of the examination (theory or practical) in which he/she is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the course of the examination)	Expulsion from the examination hall and cancellation of the performance in that course only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the examination hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he/she will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the course of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that Semester/year. The Hall Ticket of the candidate is to be cancelled.
3	Impersonates any other candidate in connection with the examination	The candidate who has impersonated shall be expelled from examination hall. The Candidate is also debarred for four consecutive semesters from class work and all end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with for feature of seat. The performance of the

		original candidate, who has been impersonated, shall be cancelled in all the courses of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that Semester/year. The candidate is also debarred for four consecutive Semesters from class work and all Semester end examinations if his involvement is established. Otherwise the candidate is debarred for two consecutive semesters from class work and all end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he/she will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that Semester/year. The candidate is also debarred for two consecutive Semesters from class work and all Semester end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that course.
6	Refuses to obey the orders of the any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walkout or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that course and all other courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the courses of that Semester.

	of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	If candidate physically assaults the invigilator or/officer in charge of the examination, then the candidate is also barred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the examination hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that Semester/year. The candidate is also debarred for two consecutive Semesters from class work and all Semester end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that Semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper	Student of the colleges expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared

	conduct mentioned in clause 6 to 8.	including practical examinations and project work and shall not be permitted for the remaining examinations of the Courses of that Semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that Semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that course and all other courses the candidate has appeared including practical examinations and project work of that Semester examinations depending on the recommendation of the committee.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Principal for further action to award suitable punishment.	

Note:

i. All malpractices cases are to be handled by the Chief Controller with a committee consist of Controller of Examinations, HOD concerned and subject expert.
ii. Whenever the performance of a student is cancelled in any course/ courses due to Malpractice, he has to register for the End Examination in those course/courses consequently and has to fulfill all the norms required for award of Degree.

COURSE STRUCTURE

M.Tech I Semester – VLSI

S.No	Course Code	Course Title	Hours per Week			Marks			Credits
			L	T	P	IM	EM	T	
1	18VL101	CMOS Analog Integrated Circuit Design	4	0	0	40	60	100	4
2	18VL102	CMOS Digital Integrated Circuit Design	4	0	0	40	60	100	4
3	**Elective-I**								
	18VL103	Hardware Description Languages	4	0	0	40	60	100	4
	18VL104	VLSI Technology and Design							
	18VL105	ASIC Design							
4	**Elective-II**								
	18VL106	DSP Processors and Architectures	4	0	0	40	60	100	4
	18VL107	Scripting language for VLSI Design Automation							
	18VL108	Algorithms for VLSI Design Automation							
5	18AS101	Research Methodology and IPR	2	0	0	40	60	100	2
6	18VL110	CMOS Analog Integrated Circuit Design Lab	0	0	4	25	50	75	2
7	18VL111	CMOS Digital Integrated Circuit Design Lab	0	0	4	25	50	75	2
		Total	**18**	**0**	**8**	**250**	**400**	**650**	**22**

M.Tech II Semester – VLSI

S.No	Course Code	Course Title	Hours per Week			Marks			Credits
			L	T	P	IM	EM	T	
1	18VL201	Embedded System Concepts	4	0	0	40	60	100	4
2	18VL202	Device Modeling	4	0	0	40	60	100	4
3	**Elective-III**								
	18VL203	FPGA Architecture and Applications	4	0	0	40	60	100	4
	18VL204	Low Power VLSI Design							
	18VL205	Real Time Operating Systems							
4	**Elective-IV**								
	18VL206	Hardware Software Co-Design	4	0	0	40	60	100	4
	18VL207	Testing and Testability							
	18VL208	RFIC Design							
5	18VL209	Mixed Signal Lab	2	0	0	40	60	100	2
6	18VL210	Embedded Processing Lab	0	0	4	25	50	75	2
7	18VL211	Term Paper	0	0	4	50	-	50	2
		Total	**18**	**0**	**8**	**275**	**350**	**625**	**22**

M.Tech III Semester – VLSI

S.No	Course Code	Course Title	Hours per Week			Marks			Credits
			L	T	P	IM	EM	T	
1		**Open Elective**	4	0	0	40	60	100	4
2	**Elective-V**								
	18VL304	Advanced Computer Architecture	4	0	0	40	60	100	4
	18VL305	System On Chip Architecture							
	18VL306	Fundamentals and Applications of MEMS							
3	18VL307	Project Work Phase-I	0	0	20	Grade			10
		Total	**8**	**0**	**8**	**80**	**120**	**200**	**18**

M.Tech IV Semester – VLSI

S.No	Course Code	Course Title	Hours per Week			Marks			Credits
			L	T	P	IM	EM	T	
1	18VL401	Project Work Phase-II	0	0	32	Grade			16
		Total	**0**	**0**	**32**	**Grade**			**16**

Open Electives – VLSI

S.No	Course Code	Course Title
1	18VL301	High Speed VLSI
2	18VL302	Nano Electronics
3	18VL303	Available MOOCs

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

M.Tech I Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL101	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. To lay good foundation on the design and analysis of CMOS analog integrated circuits.

II. In this course, transistor modeling is emphasized from a purely analog point of view. Some of the world's highest paid jobs in Electronics based industry are in Analog Circuit Design.

UNIT-I	**INTEGRATED DEVICES AND MODELING**	**Classes:10**

MOS transistors- Modeling in linear, saturation and cutoff high frequency equivalent circuit.

Integrated Devices and Modeling and Current Mirror: Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load. Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors and Bipolar Gain Stages. Frequency Response.

UNIT-II	**OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION**	**Classes:10**

Two Stage CMOS Operational Amplifier. Feedback and Operational Amplifier Compensation. Advanced Current Mirror. Folded–Cascade Operational Amplifier, Current Mirror Operational Amplifier Fully Differential Operational Amplifier. Common Mode Feedback Circuits. Current Feedback Operational Amplifier. Comparator. Charge Injection Error. Latched Comparator and Bi-CMOS Comparators.

UNIT-III	**SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS**	**Classes:10**

MOS, CMOS, Bi-CMOS Sample and Hold Circuits. Switched Capacitor Circuits: Basic Operation and Analysis. First Order and Biquard Filters.

Charge Injection. Switched Capacitor Gain Circuit. Correlated. Double Sampling Techniques. Other Switched Capacitor Circuits.

UNIT-IV	**DATA CONVERTERS**	**Classes:10**

Ideal D/A & A/D Converters. Quantization Noise. Performance Limitations. Nyquist Rate D/Converters: Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating ,Successive Approximation, Cyclic Flash Type, Two Step, Interpolating, Folding and Pipelined, A/D Converters.

UNIT-V	**OVER SAMPLING CONVERTERS AND FILTERS**	**Classes:10**

Over Sampling With and Without Noise Shaping. Digital Decimation Filter. High Order Modulators. Band Pass Over Sampling Converter. Practical Considerations. Continuous Time Filters.

Text Books:

1. D.A.John, Ken Martin, Analog Integrated Circuit Design", 1st ed., John Wiley, 1996.
2. BehzadRazavi, Design of Analog CMOS Integrated Circuit, Tata-McGrawHill, 1st ed.,2002.

Reference Books:

1. Philip Allen & Douglas Holberg, CMOS Analog Circuit Design, Oxford University Press, 3rd ed.,2011
2. GREGOLIAN &TEMES: Analog MOS Integrated Circuits, John Wiley, 1986.

Web References:

1.https://www.wiley.com/en-us/Analog+Integrated+Circuit+Design%2C+2nd+Edition-p-9780470770108

2.http://orbit.dtu.dk/files/146419573/cmos_analog_ic_design_fundamentals.pdf

E-Text Books:

1. CMOS Analog Integrated Circuit Design, Professional Publications, 2017
2. VLSI Technology and Design, Professional Publications, 2014

Outcomes:

1. Students will demonstrate the use of analog circuit analysis techniques to analyze the operation and behavior of various analog integrated circuits.
2. Students will demonstrate their knowledge by designing analog circuits
3. Design, simulation and synthesize analog circuits
4. Analyze the basic current mirrors
5. Analyze and design basic operational amplifiers
6. Understand the concept of gain, power, and bandwidth

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

M.Tech I Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL102	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. To lay good foundation on the design and analysis of CMOS digital integrated circuits.

II. To study digital circuits using various logic methods and their limitations.

UNIT-I	CMOS DESIGN	Classes:10

CMOS inverters -static and dynamic characteristics.

Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

UNIT-II	CIRCUITS AND SIZING OF TRANSISTOR	Classes:10

Method of Logical Effort for Transistor Sizing -power consumption in CMOS gates- Low power CMOS design.

Arithmetic Circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

UNIT-III	BIPOLAR GATE DESIGN	Classes:10

BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.

UNIT-IV	LAYOUT DESIGN RULES	Classes:10

Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT-V	SUBSYSTEM DESIGN PROCESS	Classes:10

General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

Text Books:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, 2nded.,MGH,1999.
2. Jan M Rabaey, Digital Integrated Circuits-ADesign Perspective,2nded.Prentice Hall,2003.
3. Eugene D Fabricus, Introduction to VLSI Design, McGraw Hill International Edition, 1990.

Reference Books:

1. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000.
2. Neil H E West and Kamran Eshranghian, Principles of CMOS VLSI Design: A System Perspective",2nd ed., Addision-Wesley,2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation,IEEE Press, 1998.
4. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital

5. Integrated Circuits, 3rd ed., McGraw-Hill, 2004

Web References:

1. https://www.u-cursos.cl/usuario/9553d43f5ccbf1cca06cc02562b4005e/mi_blog/r/CMOS_Circuit_Design__Layout__and_Simulation__3rd_Edition.pdf
2. http://www.roletech.net/books/DigitalIntegratedCircuit.pdf

E-Text Books:

1. Sung-Mo (Steve) Kang (Author), Yusuf Leblebici, McGraw-Hill Higher Education; 41 edition, 2002
2. Hubert Kaeslin, Cambridge University Press, 2008

Outcomes:

1. To study about CMOS inverters and its applications
2. To design low power CMOS circuits
3. To analyze the Bi-CMOS logic circuits
4. To study the layout design rules for designing the circuits
5. To study the static and dynamic characteristics of CMOS inverters
6. To analyze the ALU sub-system design

HARDWARE DESCRIPTION LANGUAGES
(Elective – I)

M.Tech I Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL103	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. Students can design digital circuits using a hardware description language and synthesis.

II. Students understand modern programmable logic devices and can use them in practical applications.

III. 3. Students understand timing and effects of hardware mapping and circuit parasitics.

UNIT-I	OPERATORS AND MODELING	Classes:10

Hardware Modeling with the Verilog HDL: Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

Logic System, Data Types and Operators for Modeling in Verilog HDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives – Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT-II	BEHAVIORAL AND SYNTHESIS OF VHDL	Classes:10

Behavioral Descriptions in Verilog HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

Synthesis of Combinational Logic: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares, Synthesis of Sequential Logic Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT-III	SYNTHESIS OF LANGUAGE CONSTRUCTS	Classes:10

Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

UNIT-IV	SWITCH – LEVEL MODELS IN VERILOG	Classes:10

MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

UNIT-V	BEHAVIORAL DESCRIPTION OF HDL	Classes:10

Introduction to HDL: An Overview of Design Procedures used for System Design using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. Design Verification Tools. Examples using Commercial PC Based on VHDL Elements of VHDL Top Down Design with VHDL Subprograms. Controller Description VHDL Operators.

Behavioral Description of Hardware in HDL: Process Statement Assertion Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design. Differences between VHDL and Verilog.

Text Books:

1. M.D.CILETTI, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice-Hall, 1999.
2. Z.NAWABI, VHDL Analysis and Modeling of Digital Systems, 2nd ed., McGraw Hill, 1998.

Reference Books:

1. M.G.ARNOLD, Verilog Digital – Computer Design, Prentice-Hall (PTR), 1999.
2. PERRY, VHDL, 3rd ed., McGraw Hill.

Web References:

1. https://en.wikipedia.org/wiki/Hardware_description_language
2. https://www.allaboutcircuits.com/technical-articles/hardware-description-langauge-getting-started-vhdl-digital-circuit-design/

E-Text Books:

1. Douglas L. Perry, VHDL Programming by Example, Mc-Graw Hill, 2002
2. VA Pedroni, Circuit Design with VHDL, Library of Congress Cataloging-in-Publication, 2004

Outcomes:

1. Understand verilog program structures
2. Understand gate level and switch level modeling
3. Design various program descriptions
4. Design digital systems using simple and moderately complex systems using methodologies that are common for the implementation to reconfigurable logic devices.
5. Use typical design techniques for combinational circuits, asynchronous and synchronous state machines and busses.
6. Implement the process of synthesis and post-synthesis in the developed systems and verify their functioning once implemented in reconfigurable logic devices.

VLSI TECHNOLOGY AND DESIGN
(Elective – I)

M.Tech I Semester: VLSI

Course code	Category	Hours/week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	TOTAL
18VL104	Core	4	-	-	4	40	60	100
Contact Classes:50	Tutorial Classes: -	Practical Classes: Nil			Total Classes:50			

OBJECTIVES:

The course should enable the students to :

I. To learn the basic MOS Circuits
II. To learn the MOS Process Technology
III. To understand the operation of MOS devices.
IV. To impart in-depth knowledge about analog and digital CMOS circuits

UNIT-I INTRODUCTION — **Classes:10**

Review of Microelectronics and Introduction to MOS Technologies: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

Basic Electrical Properties of MOS, CMOS & BICOMS Circuits: Ids -Vds Relationships, Threshold Voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, Zpu/Zpd, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT-II LAYOUT DESIGN — **Classes:10**

Layout Design and Tools: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT-III COMBINATIONAL LOGIC NETWORKS — **Classes:10**

Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT-IV SEQUENTIAL SYSTEMS — **Classes:10**

Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT-V DESIGN AND PLANNING — **Classes:10**

Floor Planning & Architecture Design: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

Introduction to CAD Systems (Algorithms) and Chip Design: Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

Text Books:

1. K. Eshraghianet . al(3 authors), Essentials of VLSI Circuits and Systems, , PHI of India Ltd.,2005
2. Wayne Wolf, Modern VLSI Design, 3rd ed., Pearson Education,2005.

Reference Books:

1. N.H.E Weste, K.Eshraghian, Adison Wesley, Principals of CMOS Design, 2nd ed.,1993
2. Fabricius, Introduction to VLSI Design, MGH International Edition, 1990.

3. Baker, Li Boyce, CMOS Circuit Design, Layout and Simulation, PHI, 2004.

Web References:

1. http://www.csit-sun.pub.ro/courses/vlsi/Modern_VLSI_Design.pdf
2. https://electronicsforu.com/resources/learn-electronics/vlsi-developments-ic-fabrication

E-Text Books:

1. Wayne wolf, Prentice Hall, 2008
2. Pucknell and Eshraghian, Basic VLSI Design, 2004

Outcomes:

1. To be aware about the trends in semiconductor technology, and how it impacts scaling and performance
2. To understand MOS transistor as a switch and its capacitance
3. learn Layout, Stick diagrams, Fabrication steps, Static and Switching characteristics of inverters
4. Design, built and debug complex combinational and sequential circuits based on an abstract functional specification.
5. Synthesis of digital VLSI systems from register-transfer or higher level descriptions in hardware design languages.
6. Student will be able to design digital systems using MOS circuits.

ASIC DESIGN
(Elective – I)

M.Tech I Semester: VLSI								
Course code	Category	Hours/week			Credits	Maximum Marks		
18VL105	Core	L	T	P	C	CIA	SEE	TOTAL
		4	-	-	4	40	60	100
Contact Classes:50	Tutorial Classes: -	Practical Classes: Nil				Total Classes:50		

OBJECTIVES:

The course should enable the students to :

I. To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.

II. To give the student an understanding of issues and tools related to ASIC/FPG A design and implementation.

III. To give the student an understanding of basics of System on Chip and Platform based design

UNIT-I	INTRODUCTION TO ASIC	Classes:10

ASIC Design Styles: Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs.

ASICS – Programmable Logic Devices: Overview – PAL –based PLDs: Structures; PAL Characteristics – FPGAs: Introduction, selected families – design outline.

UNIT-II	DESIGN METHODOLOGIES	Classes:10

ASICS –Design Issues: Design methodologies and design tools – design for testability – economies.

ACISS Characteristics and Performance: design styles, gate arrays, standard cell -based ASICs, Mixed mode and analogue ASICs.

UNIT-III	ASICS-DESIGN TECHNIQUES	Classes:10

Overview- Design flow and methodology-Hardware description languages-simulation and checking-commercial design tools-FPGA Design tools: XILINX, ALTERA

UNIT-IV	LOGIC SYNTHESIS, SIMULATION AND TESTING	Classes:10

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation- automatic test pattern generation

UNIT-V	CONSTRUCTION AND PARTIOINING	Classes:10

ASIC Construction: Floor planning, placement and routing system partition.

FPGA Partitioning: Partitioning Methods-Floor Planning- Placement-Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

Text Books:

1. L.J.Herbst, Integrated Circuit Engineering, OXFORD SCIENCE Publications, 1996.

Reference Books:

1. M.J.S.Smith, Application - Specific integrated circuits, Addison-Wesley Longman Inc ,1997.

Web References:

1. https://en.wikipedia.org/wiki/Application-specific_integrated_circuit

2.http://www.asic-world.com/

E-Text Books:

1. Norman G. Einspruch, Jeffrey L. Hilbert, Application Specific Integrated Circuit (ASIC)

Technology, Academic Press, 1991

2. Ashok B. Mehta, ASIC/SoC Functional Design Verification, Springer International Publishing; June 2017

Outcomes:

1. Demonstrate in-depth knowledge in ASIC Design Styles, ASICs Design Issues, ASICs Design Techniques, ASIC Construction.
2. Analyze the characteristics and Performance of ASICs and judge independently the best suited device for fabrication of smart devices for conducting research in ASIC design.
3. Solve problems of Design issues, simulation and Testing of ASICs.
4. Apply appropriate techniques, resources and tools to engineering activities for appropriate Solution to develop ASICs.
5. Understand different FPGA Partitioning methods

DSP PROCESSORS AND ARCHITECTURES
(Elective – II)

M.Tech I Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL106	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. To give an exposure to the various fixed point & a floating point DSP architectures

II. To develop applications using these processors.

UNIT-I INTRODUCTION **Classes:10**

Introduction,Digitalsignal-processingsystem, Thesamplingprocess, Discretetimesequences.DiscreteFourierTransform(DFT)andFast FourierTransform(FFT),Lineartime-invariantsystems,Digitalfilters, Decimation andinterpolation, Analysis and Design tool for DSP SystemsMATLAB,DSPusingMATLAB.

ComputationalAccuracyinDSPImplementations:

Number formatsforsignalsandcoefficientsinDSPsystems,Dynamic RangeandPrecision,SourcesoferrorinDSPimplementations, A/D Conversionerrors,DSPComputational errors,D/AConversionErrors, Compensatingfilter.

UNIT-II ARCHITECTURES AND EXECUTION **Classes:10**

ArchitecturesforProgrammableDSPDevices:

BasicArchitecturalfeatures,DSPComputationalBuildingBlocks,Bus Architecture and Memory, Data Addressing Capabilities, Address Generationunit, ProgrammabilityandProgramExecution,Speed Issues, FeaturesforExternalinterfacing.

ExecutionControlandPipelining:

Hardware looping, Interrupts, Stacks, Relative Branch support, PipeliningandPerformance,PipelineDepth,Interlocking,Branching effects,Interrupteffects,PipelineProgrammingmodels.

UNIT-III IMPLEMENTATION OF DSP **Classes:10**

ProgrammableDigitalSignalProcessors:

CommercialDigitalsignal-processingDevices,DataAddressingmodes ofTMS320C54XXDSPs,DataAddressingmodesofTMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control,TMS320C54XX instructionsandProgramming,On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline OperationofTMS320C54XXProcessors.

ImplementationsofBasicDSPAlgorithms:

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters,DecimationFilters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT-IV IMPLEMENTATION OF FFT ALGORITHMS **Classes:10**

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT-V	INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES	Classes:10

Memoryspaceorganization,Externalbusinterfacingsignals,Memory interface,ParallelI/Ointerface,ProgrammedI/O,InterruptsandI/O, Directmemoryaccess(DMA). AMultichannelbufferedserialport(McBSP),McBSPProgramming,a CODEC interfacecircuit, CODEC programming, A CODEC-DSP interfaceexample.

Text Books:

1. Avtar Singh and S. Srinivasan, Digital Signal Processing, Thomson Publications, 2004.
2. Lapsleyetal, DSP Processor Fundamentals, Architectures & Features, S.Chand& Co, 2000.

Reference Books:

1. B. VenkataRamani, M. Bhaskar, Digital Signal Processors, Architecture, Programming and Applications, 4th ed. Reprint,TMH,2008.
2. Jonatha Stein, Digital Signal Processing ,1st ed., John Wiley, 2005

Web References:

1. https://en.wikipedia.org/wiki/Digital_signal_processor
2.https://ieeexplore.ieee.org/document/6771184

E-Text Books:

1. Kuo, Digital Signal Processors: Architectures, Implementations, and Applications, Pearson Education India, 2005
2. Phil Lapsley, Jeff Bier, AmitShoham, Edward A. Lee, DSP Processor Fundamentals: Architectures and Features, Wiley India Pvt Ltd, 2009.

Outcomes:

1. Comprehends the knowledge & concepts of digital signal processing techniques.
2. Learn the DSP programming tools and use them for applications
3. Students will be able to use the DSP processors TMS 320C 54XX for implementation of DSP algorithms & its interfacing techniques with various I/O peripherals.
4. Students will be able to use MATLAB DSP toolbox for analysis & design of DSP.
5. Acquire knowledge of DSP computational building blocks and knows how to Achieve speed in DSP architecture or processor.
6. Learn the architecture details and instruction sets of fixed and floating point DSPs

SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION
(Elective – II)

M.Tech I Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL107	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. Understand the complexities and design methodologies of VLSI/nanometer scale IC and ASIC design methodologies.

II. Apply advanced technologies in the fields of VLSI design along with the fundamental concepts.

III. Use techniques, skills, modern Electronic Design Automation(EDA) tools, software and equipment necessary to evaluate and analyze the systems in VLSI design environments.

IV. Facilitate the students using industry standard EDA tools and adopt sign-off design methodology for realizing complex VLSI systems for a given specification

UNIT-I	**OVERVIEW OF SCRIPTING LANGUAGES**	**Classes:10**
PERL, CGI, VB Script, Java Script.		
UNIT-II	**PERL**	**Classes:10**
Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.		
UNIT-III	**COMMUNICATION THREADS**	**Classes:10**
Inter process Communication Threads, Compilation & Line Interfacing.		
UNIT-IV	**PROGRAMMING IN PERL**	**Classes:10**
Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL		
UNIT-V	**OTHER LANGUAGES**	**Classes:10**
Broad Details of CGI, VB Script, Java Script with Programming Examples		

Text Books:

1. Randal L, Schwartz Tom Phoenix, Learning PERL, 3rd ed., Oreilly Publications, 2000
2. Larry Wall, Tom Christiansen, John Orwant, Programming PERL, 3rd ed., Oreilly Publications 2000.
3. Tom Christiansen, Nathan Torkington, PERL Cookbook, 3rd ed., Oreilly Publications, 2000.

Reference Books:

1. VLSI Design-Dr.K.V.K.K.Prasad, KattulaShyamala, Kogent Learning Solutions Inc., 2012
2. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2nd Edition, Addison Wesley

Web References:

1. http://tech.asj-oa.am/3949/4/350.pdf

E-Text Books:

1. Micheal L. Schott, Programming Level Pragmatics, Morgan Kauffman Publishers, 2006

Outcomes:

1. Learn concepts of PERL, CGI, VB Script, Java Script.
2. Analyze PERL Pattern Matching, Data Structures, Modules, Objects, Tied Variables.
3. Understand the Inter process Communication Threads
4. Identify the various Portable Functions and Extensive Exercises for Programming in PERL .
5. Study of VB Script, Java Script with Programming Examples

ALGORITHMS FOR VLSI DESIGN AUTOMATION
(Elective – II)

M.Tech I Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL108	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
II. Discuss the concepts of design optimization algorithms and their application to physical design automation.
III. Understand the concepts of simulation and synthesis in VLSI Design Automation
IV. Formulate CAD design problems using algorithmic methods

UNIT-I	INTRODUCTION	Classes:10

Preliminaries: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

General Purpose Methods for Combinational Optimization: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT-II	MODELLING AND SIMULATION	Classes:10

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT-III	LOGIC SYNTHESIS AND VERIFICATION	Classes:10

Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

High – Level Synthesis: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT-IV	PHYSICAL DESIGN AUTOMATION OF FPGA'S	Classes:10

FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT-V	PHYSICAL DESIGN AUTOMATION OF MCM'S	Classes:10

MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin, Distribution and routing, Routing and Programmable MCM's.

Text Books:

1. S.H.Gerez, Algorithms for VLSI Design Automation, WILEY Student Edition, John wiley& Sons (Asia) Pvt. Ltd., 1999
2. NaveedSherwani, Algorithms for VLSI Physical Design Automation ,3rd ed., Springer International edition, 2005

Reference Books:

1. Hill & Peterson, Computer Aided Logical Design with Emphasis on VLSI, Wiley, 1993.
2. Wayne Wolf, Modern VLSI Design Systems on silicon, 2nd ed., Pearson Education Asia, 1998

Web References:

1. https://doc.lagout.org/science/0_Computer%20Science/2_Algorithms/Algorithms%20for%20VLSI%20Design%20Automation%20%5BGerez%201998-12-22%5D.pdf
2. http://cc.ee.ntu.edu.tw/~ywchang/Courses/EDA/lec1.pdf

E-Text Books:

1. S.M. Sait , H. Youssef, "VLSI Physical Design Automation", World scientific, 1999.
2. M.Sarrafzadeh, "Introduction to VLSI Physical Design", McGraw Hill (IE), 1996.

Outcomes:

1. Ability to model automation of VLSI design.
2. Ability to apply optimization techniques to the process of VLSI design.
3. Understand the layout compaction, modeling and simulation.
4. Learn the concepts of logic and high level synthesis and verification.
5. Analyze the physical design Automation of FPGA and MCM'S

RESEARCH METHODOLOGY AND IPR

M.Tech I Semester: Common to all Branches								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18AS101	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	0	0	4	40	60	100
Contact Classes:60	**Tutorial Classes: -**		**Practical Classes: Nil**			**Total Classes:60**		

OBJECTIVES:

The course should enable the students to:

1. Understand research problem formulation.
2. Analyze research related information
3. Follow research ethics
4. Understand that today's world is controlled by computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
5. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
6. Understand the IOR protection provides an incentive to inventors for further research work and investment in R&D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT-I — **Classes:12**

Research Methodology:

Meaning of research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowledge how Research is done, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India.

Research Design:

Meaning of Research Design, Need for Research Design, Features of Good Design, Important concepts relating to Research Design, Different Research Designs, Basic principles of experimental designs.

UNIT-II — **Classes:12**

Methods of Data Collection:

Collection of Primary Data, Observation Method, Interview Method, Collection of Data through Questionnaires, Collection of Data through Schedules, Difference between Questionnaires and Schedules, Some other methods of data collection, Collection of secondary data, Selection of appropriate method for data collection, Case study method.

UNIT-III — **Classes:12**

Testing of Hypotheses:

What is a Hypothesis, Basic concepts concerning testing of hypothesis, Procedure for hypothesis testing, Flow diagram for hypothesis testing, Measuring the power of a hypothesis test, Tests of hypotheses, Importance of Parametric Tests, Hypothesis testing of means, Hypothesis testing for differences between means, Hypothesis testing for comparing two related samples, Hypothesis testing of proportions, Hypothesis testing for difference between proportions, Hypothesis testing for comparing a variance some hypothesized population variance, Testing and equality of variances of two normal populations, Hypothesis testing of correlation coefficients, Limitations of the tests of Hypotheses.

UNIT-IV	Classes:12

Interpretation and Report Writing:

Meaning of Interpretation, Why Interpretation?, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different steps in writing report, Layout of the Research Project, Types of reports, Oral presentation, Mechanics of writing a research report, Precautions for writing research reports.

UNIT-V	Classes:12

Intellectual Property Rights:

Module I- Introduction

1) Intellectual property: meaning, nature and significance
2) Various forms of intellectual properties: copyright, patent, trademark, design, geographical indication, semiconductor and plant variety
3) Major international instruments relating to the protection of intellectual properties

Module II- Copyright

1) Copyright: meaning ,scope
2) Subject matter of copyright: original literary, dramatic, musical, artistic works; cinematograph films and sound recordings
3) Ownership of copyright , Assignment and licence of copyright
4) Infringement and exceptions of infringement of copyright and remedies against infringment of copyright: civil, criminal and administrative.

Module III – Trade Marks

1. Trade mark: meaning,scope
2. Absolute and relative grounds of refusal
3. Doctrine of honest concurrent user
4. Procedure for registration and term of protection
5. Rights of holder and assignment and licensing of marks
6. Infringement and remedies
7. Trade marks registry and appellate board

Module IV- Patents

1. Patent: meaning
2. Criteria for patentability and non-patentable inventions
3. Procedure for registration and term of protection
4. Grants of patent, rights of patentee and revocation of patent
5. Compulsory licence and government use of patent
6. Infringement, exceptions to infringement of patent and remedies
7. Patent office and Appellate Board

Text Books

1. Kothari. C.R, 1990,"Research methodology: Methods and Techniques. New Age International, 418P
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A step by Step Guide for beginers"

Reference Books:

1. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd. 2007
2. Mayall, "Industrial Design", McGraw Hill, 1974.
3. Niebel, "Product Design", McGraw Hill, 1974.
4. Asimov, "Introduction to Design", Prentice Hall, 1962.
5. Robert P.Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.
6. T.Ramappa, "Intellectual Property Rights Under WTO", S.Chand, 2008

CMOS ANALOG INTEGRATED CIRCUIT DESIGN LABORATORY

M.Tech I Semester – VLSI

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
18VL110	Core	-	-	4	2	25	50	75
Contact Classes: Nil	Tutorial Classes: Nil		Practical Classes: 39			Total Classes: 39		

OBJECTIVES:

The course should enable the students to:

I. To lay good foundation on the design and analysis of CMOS analog integrated circuits.
II. In this course, transistor modeling is emphasized from a purely analog point of view. Some of the world's highest paid jobs in Electronics based industry are in Analog Circuit Design.

LIST OF EXPERIMENTS

Expt. 1 **NMOS INVERTER**

Depletion and Enhancement Mode Circuit Simulation and Adjustment of Vh VLSI Vm parameters for NMOS inverter.

Expt. 2 **CMOS INVERTER**

Circuit Simulation, adjustment of W / L ratio of P & N channel MOS transistor for symmetrical drive output and loading consideration. Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners).Layout of CMOS Inverter, Extraction of parasitic and back annotation and related modifications in circuit parameters and layout.

Expt. 3 **CURRENT SOURCE / MIRROR**

Circuit simulation of current Mirror using BJT and MOS(Simple, Wilson and Wilder configurations) study and modifications to improve power and load regulation. Layout of CMOS Current Mirror.

Expt. 4 **8 BIT SHIFT REGISTER CELL**

Building of cell Library of logic gates and flip flops and building of 8 bit shift register from the same. Optimization of the same from layout and power considerations.

Expt. 5 **DIFFERENTIAL AMPLIFIER**

Study of specifications of Differential amplifier and Design considerations. Study of input loading and biasing techniques.

Reference Books:

1. Philip Allen & Douglas Holberg, CMOS Analog Circuit Design, Oxford University Press, 3rd ed.,2011
2. GREGOLIAN &TEMES: Analog MOS Integrated Circuits, John Wiley, 1986.

Web References:

1. https://www.wiley.com/en-us/Analog+Integrated+Circuit+Design%2C+2nd+Edition-p-9780470770108
2. http://orbit.dtu.dk/files/146419573/cmos_analog_ic_design_fundamentals.pdf

Course Home Page:

SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 36 STUDENTS:

SOFTWARE: Mentor Graphic tools / Cadence tools/ Synopsys's tools/Microwind. (180 nm Technology and Above)

HARDWARE: Desktop Computers (04 nos)

Course Outcome:

At the end of the course, a student will be able to:

1. Model NMOS inverter
2. Design and simulate CMOS inverter with W/L ratio
3. Produce layout of CMOS inverter and extract parasitic elements
4. Familiarize the design of current source mirror using BJT and MOS
5. Study the design of differential amplifier and to extract the design outcome.

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN LABORATORY

M.Tech I Semester – VLSI

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
18VL110	Core	-	-	4	2	25	50	75
Contact Classes: Nil	Tutorial Classes: Nil	Practical Classes: 39			Total Classes: 39			

OBJECTIVES:

The course should enable the students to:

I. To lay good foundation on the design and analysis of CMOS digital integrated circuits.
II. To study digital circuits using various logic methods and their limitations.

LIST OF EXPERIMENTS

Expt. 1	**DIGITAL CIRCUITS DESCRIPTION USING VERILOG AND VHDL.**
This Experiment focus on different HDL's	
Expt. 2	**VERIFICATION OF THE FUNCTIONALITY OF DESIGNED CIRCUITS USING FUNCTION SIMULATOR**
This Experiment focus on functionality using simulator	
Expt. 3	**TIMING SIMULATION FOR CRITICAL PATH TIME CALCULATION**
This Experiment focus on timing simulation	
Expt. 4	**PLACE AND ROUTE TECHNIQUES FOR MAJOR FPGA VENDORS SUCH AS XILINX, ALTERA AND ACTEL**
This Experiment focus on placing and routing	
Expt. 5	**IMPLEMENTATION OF DESIGNED DIGITAL CIRCUITS USING FPGA AND CPLD DEVICES**
This Experiment focus on implementation of digital circuits	

Reference Books:

1. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000.
2. Neil H E West and Kamran Eshranghian, Principles of CMOS VLSI Design: A System Perspective",2nd ed., Addision-Wesley,2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation,IEEE Press, 1998.
4. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital
5. Integrated Circuits, 3rd ed., McGraw-Hill, 2004

Web References:

1. https://www.u-cursos.cl/usuario/9553d43f5ccbf1cca06cc02562b4005e/mi_blog/r/CMOS_Circuit_Design__Layout__and_Simulation__3rd_Edition.pdf
2. http://www.roletech.net/books/DigitalIntegratedCircuit.pdf

Course Home Page:
SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 36 STUDENTS: **SOFTWARE:**Mentor Graphic tools / Cadance tools/ Synophysis tools. (180 nm Technology and Above) **HARDWARE:** Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.
Course Outcome: At the end of the course, a student will be able to: 1. Apply theory and practice for designing digital logic circuits and logic system designs 2. Familiarize with the VHDL using Xilinx 3. Verify the design logic of combinational and sequential circuit 4. Simulate timing analysis and to calculate critical path time 5. Programming on FPGA for different digital logic circuits

EMBEDDED SYSTEM CONCEPTS

M.Tech II Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL201	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. To introduce students to the modern embedded systems and to show how to understand and program such systems using a concrete platform built around

II. A modern embedded processor like the Intel ATOM.

UNIT-I	INTRODUCTION	Classes:10

Introduction to Embedded Systems: An Embedded System, Processor in The System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System -On-Chip (SOC) and in VLSI Circuit.

Processor and Memory Organization: Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

UNIT-II	DEVICES AND BUSES FOR DEVICE NETWORKS	Classes:10

I/O Devices, Timer and Counting Devices, Serial Communication Using The "I^2C" , CAN, Profibus Foundation Field Bus. and Advanced I/O Buses Between the Network Multiple Devices, Host Systems or Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses.

UNIT-III	DEVICE DRIVERS AND INTERRUPTS SERVICING MECHANISM	Classes:10

Device Drivers, Parallel Port and Serial Port Device Drivers in a System, Device Drivers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

UNIT-IV	PROGRAMMING CONCEPTS	Classes:10

Instruction Sets: Introduction, preliminaries, ARM processor, SHARC processor.

Embedded Programming in C, C++, VC++ and JAVA: Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

UNIT-V	HARDWARE- SOFTWARE C0- DESIGN IN AN EMBEDDED SYSTEM	Classes:10

Embedded System Project Management, Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, use of Target Systems, use of Software Tools for Development of an Embedded System, use of Scopes and Logic Analysis for System, Hardware Tests. Issues in Embedded System Design.

Text Books:

1. Rajkamal, Embedded systems: Architecture, Programming and Design, TMH, 2008.
2. Wayne wolf, Computers as a component: principles of embedded computing system design.

Reference Books:

1. Arnold S Berger, Embedded System Design, 1st ed., CMP Books, 2001.
2. An embedded software primer by David Simon, 1st Indian Reprint, PEA, 2001.
3. Steve Heath, Embedded systems design: Real world design , Newton Mass USA, 2002.

Web References:

1. https://www.slideshare.net/yayavaram/introduction-to-embedded-systems-2614825
2. https://pdfs.semanticscholar.org/a24e/c6903e740a61af9310efda3b7af8cdd00401.pdf

E-Text Books:

1. Qing Li, Caroline Yao, Real-Time Concepts for Embedded Systems, CRC Press, 2003.
2. Barrett, Embedded Systems: Design and Applications, Pearson Education, 2008.

Outcomes:

1. Describe the differences between the general computing system and the embedded system, also recognize the classification of embedded systems..
2. Design real time embedded systems using the concepts of RTOS.
3. To understand the processor and memory organization in an embedded system.
4. To learn the basic instruction set of ARM, SHARC processor and programming concepts.
5. To study devices and buses used in embedded system.
6. To understand the concept of Hardware- Software C0- Design in an Embedded System

DEVICE MODELING

M.Tech II Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
		L	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
18VL202	**Core**	4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. To understand operation of semiconductor devices.
II. To understand DC analysis and AC models of semiconductor devices.
III. To implement mini projects based on concept of electronics circuit concepts.

UNIT-I	INTRODUCTION	Classes:10

Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures.

UNIT-II	INTEGRATED DIODES AND TRANSISTOR	Classes:10

Integrated Diodes: Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models.

Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model- dynamic model, Parasitic effects – SPICE model – Parameter extraction.

UNIT-III	INTEGRATED MOS TRANSISTOR	Classes:10

NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4.

UNIT-IV	VLSI FABRICATION TECHNIQUES	Classes:10

An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements.

UNIT-V	MODELING OF HETERO JUNCTION DEVICES	Classes:10

Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe.

Text Books:

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

Reference Books:

1. Sze S. M, Physics of Semiconductor Devices, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Tor A. Fijedly , Introduction to Device Modeling and Circuit Simulation, Wiley-Interscience, 1997
3. Ming-BO Lin, Introduction to VLSI Systems: A Logic, Circuit and System Perspective, CRC Press, 2011

Web References:

1. https://en.wikipedia.org/wiki/Semiconductor_device_modeling

2. https://pdfs.semanticscholar.org/16a0/29541c2889de936e3e0e1d338d06ed485263.pdf

E-Text Books:

1. C. Snowden, Introduction to semiconductor device modeling, World Scientific, 1998.

Outcomes:

1. Develop solution to overcome short channel issues
2. Develop compact models appropriate for industry
3. Analyze current distribution in the devices like transistors and MOS devices
4. Understand different types of spice modeling's
5. Understand different fabrication techniques
6. Understand the Eber-Moll, Gunmel - Poon bipolar model

FPGA ARCHITECTURE AND APPLICATIONS
(Elective – III)

M.Tech II Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL203	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. Familiarization of various complex programmable Logic devices of different families.
II. To study Field programmable gate arrays and realization techniques.
III. To study different case studies using one hot design methods.

UNIT-I	INTRODUCTION	Classes:10

Programmable Logic: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

FPGA: Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

UNIT-II	FINITE STATE MACHINES(FSM)	Classes:10

Case Studies: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance. Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

UNIT-III	REALIZATION OF STATE MACHINE	Classes:10

Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT-IV	FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN	Classes:10

Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

UNIT-V	DIGITAL FRONT END DIGITAL DESIGN TOOLS FOR FPGAS & ASICS	Classes:10

Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

Text Books:

1. P.K.Chan& S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall, 1994.
2. S.Trimberger , Field Programmable Gate Array Technology, Kluwer Academic Publications,1994.

Reference Books:

1. John V. Oldfield, Richard C. Dorf, "Field Programmable Gate Arrays", Wiley India.

Web References:

1. https://www.edgefx.in/fpga-architecture-applications/
2. https://en.wikipedia.org/wiki/Field-programmable_gate_array

E-Text Books:

1. Christophe Bobda, Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications, Springer, 2010.

Outcomes:

1. Able to gain the knowledge about PLDs, FPGA Design & architectures.
2. Students should be able to understand different types of FSM's
3. Different FSM techniques like ASM and One-hot Design method
4. Understand the various frontend design tools and implementation process.
5. Analyze System level Design and their application for Combinational and Sequential Circuits.

LOW POWER VLSI DESIGN
(Elective – III)

M.Tech II Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL204	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. Familiarization of various complex programmable Logic devices of different families.
II. To study Field programmable gate arrays and realization techniques.
III. To study different case studies using one hot design methods.

UNIT-I	INTRODUCTION	Classes:10

Low Power Design, an Over View: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS Processes: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT-II	DEVICE BEHAVIOR AND MODELING	Classes:10

Low-Voltage/Low Power CMOS/ BICMOS Processes: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT-III	LOGIC GATES	Classes:10

CMOS and Bi-CMOS Logic Gates: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

Low- Voltage Low Power Logic Circuits: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation

UNIT-IV	LOW POWER LATCHES AND FILIP FLOPS	Classes:10

Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT-V	SPECIAL TECHNIQUES	Classes:10

Power Reduction in Clock Networks, CMOS Floating Node,Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

Text Books:

1. Yeo Rofail/ Gohl(3 Authors), "CMOS/BiCMOS ULSI low voltage, low power", Pearson Education Asia, 1st Indian reprint,2002.
2. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP, 2002.

Reference Books:

1. Douglas A.Pucknell& Kamran Eshraghian, Basic VLSI Design, 3rd ed., PHI, 2005.
2. J.Rabaey, Digital Integrated circuits, PHI,1996
3. Sung-mo Kang and Yusuf Leblebici, CMOS Digital ICs, 3rd ed., TMH 2003.
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia

Web References:

1. https://pdfs.semanticscholar.org/921c/9c904a79f91b85a4b086cb446c4d33911c3c.pdf
2. http://www.eecg.toronto.edu/~jayar/pubs/brown/survey.pdf

E-Text Books:

1. A. ArockiaBazil Raj, FPGA-Based Embedded System Developer's Guide, and Applications, CRC Press, 2018.
2. Christian De Schryver, FPGA Based Accelerators for Financial Applications, Springer, 2016.

Outcomes:

1. Trends in semiconductor technology, and how it impacts scaling and performance.
2. Low-power design concepts and voltage-frequency scaling.
3. Understand different isolation techniques in BICMOS technology
4. design deep-submicron silicon technologies, high performance simulation models likewise hspice, pspice.
5. Apply in practice technology-level, circuit-level, and system-level power optimization techniques.
6. Design different high performance digital circuits, optimization theme, performance theme.

REAL TIME OPERATING SYSTEMS
(Elective – III)

M.Tech II Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL205	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. To learn the fundamentals of Operating Systems

II. To know the components and management aspects of Real time, Mobile operating Systems.

UNIT-I	INTRODUCTION	Classes:10

Introduction to UNIX: Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

Real Time Systems: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

UNIT-II	APPROACHES TO REAL TIME SCHEDULING	Classes:10

Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

UNIT-III	OPERATING SYSTEMS	Classes:10

Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

UNIT-IV	CASE STUDIES	Classes:10

Fault Tolerance Techniques: Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

Case Studies – VX Works: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

UNIT-V	RT LINUX	Classes:10

Process Management, Scheduling, Interrupt Management, and Synchronization

Text Books:

1. Richard Stevens, Advanced Unix Programming, 2nd ed., Addison-Wesley, 2005.
2. Jane W.S. Liu, Real Time Systems, 1st ed., Pearson Education, 2000
3. C.M.Krishna, KANG G. Shin, Real Time Systems, McGraw.Hill, 1997

Reference Books:

1. Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
2. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley.

Web References:

1. https://en.wikipedia.org/wiki/Operating_system

E-Text Books:

1. Silberschatz, Galvin, Gagne: Operating System Concepts, 8th Edition, Wiley, 2008
2. Andrew S. Tanenbaum, Albert S. Woodhull: Operating Systems, Design and Implementation, 3rd Edition, Prentice Hall, 2006.
3. Pradeep K Sinha: Distribute Operating Systems, Concept and Design, PHI, 2007

Outcomes:

1. To distinguish a real-time system from other systems.
2. To identify the functions of operating system.
3. To evaluate the need for real-time operating system.
4. To implement the real-time operating system principles.
5. To analyze the case studies like VX works, RT Linux.
6. To understand the fault tolerance techniques in real time operating systems.

HARDWARE SOFTWARE CO-DESIGN
(Elective – IV)

M.Tech II Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL206	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. Analyze and explain the control-flow and data-flow of a software program and a cycle-based hardware description,

II. Transform simple software programs into cycle-based hardware descriptions with equivalent behavior and vice versa,

III. Partition simple software programs into hardware and software components, and create appropriate hardware-software interfaces to reflect this partitioning,

IV. Identify performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software components, and

V. Use simulation software to co-simulate software programs with cycle-based hardware descriptions.

UNIT-I	CO-DESIGN AND SYNTHESIS	Classes:10

Co-Design Issues: Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware- software partitioning distributed system co-synthesis.

UNIT-II	PROTOTYPING AND EMULATION	Classes:10

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

UNIT-III	TARGET ARCHITECTURES	Classes:10

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8050-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-IV	COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR	Classes:10

Architectures: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT-V	LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN	Classes:10

System – level specification, design representation for system level synthesis, system level specification languages, Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

Text Books:

1. Jorgen Staunstrup, Wayne Wolf, Hardware / software co- design Principles and Practice, springer,2009.
2. Hardware / software co- design Principles and Practice, Kluwer Academic Publishers , 2002.

Reference Books:

1. Wayne Wolf, Readings in hardware/software co-design, Kluwer Academic Publishers., 2001.

Web References:

1. https://books.google.co.in/books/about/Hardware_Software_Co_Design_for_Data_Flo.html?id=ZHdId5u0GCYC&redir_esc=y
2. https://ieeexplore.ieee.org/document/6172642

E-Text Books:

1. DeMicheli, Giovanni, Sami, Mariagiovanna, Hardware/Software Co-Design, Springer, 2006
2. Patrick R. Schaumont, A Practical Introduction to Hardware/Software Codesign, 3rd Edition, Springer, 2010.

Outcomes:

1. Analyze hardware-software co-design problems for systems with moderate complexity.
2. Apply hardware-software co-design methods and techniques to practical problems.
3. Designing hardware-software co-design solutions through SoPC and similar technologies.
4. Applying different levels of abstractions and provide models for verification of the architecture and functionality for embedded co-design solutions.
5. Evaluate and compare quality solutions compared to for example: performance, cost, security, power consumption and size.
6. Partition and design space exploration with LYCOS

TESTING AND TESTABILITY
(Elective – IV)

M.Tech II Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL207	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.

UNIT-I	INTRODUCTION	Classes:10

Introduction to Test and Design for Testability (DFT) Fundamentals: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

Fault Modeling: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

UNIT-II	TESTING FOR SINGLE STUCK FAULTS (SSF)	Classes:10

Automated Test Pattern Generation (ATPG/ATG) For Ssfs In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models. Vector Simulation – ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

UNIT-III	DESIGN FOR TESTABILITY	Classes:10

Testability Trade-Offs, Techniques. Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design. Board Level and System Level DFT Approaches. Boundary Scans Standards. Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT-IV	BUILT – IN SELF – TEST (BIST)	Classes:10

BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT-V	BRIEF IDEAS ON EMBEDDED CORE TESTING	Classes:10

Memory BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

Text Books:

1. MironAbramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, 1st ed., Jaico Publishing House, 2001.

Reference Books:

1. Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall, 1999.
2. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, 1998.

Web References:

1. http://www0.cs.ucl.ac.uk/staff/M.Harman/wse09.pdf
2. https://en.wikipedia.org/wiki/Design_for_testing

E-Text Books:

1. N. Jha& S.D. Gupta, Testing of Digital Systems, Cambridge, 2003.
2. W. W. Wen, VLSI Test Principles and Architectures Design for Testability, Morgan Kaufmann Publishers, 2006

Outcomes:

1. To study the modeling of digital circuits
2. To analyze the fault detection and fault correction
3. To analyze the fault modeling
4. To design the testing of single stuck faults
5. To design the built in self test (BIST) circuits
6. To study about Memory BIST (MBIST) and embedded core testing

RFIC DESIGN
(Elective – IV)

M.Tech II Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL208	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. Design monolithic inductors for integrated amplifiers and oscillators.

II. Design IC implementations of RF functional blocks (such as amplifiers, mixers and oscillators) based on foundry models and design rules to meet specifications for a wireless communications system.

UNIT-I	INTRODUCTION	Classes:10

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology.

BASIC CONCEPTS IN RF DESIGN: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT-II	MULTIPLE ACCESS	Classes:10

Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards.

UNIT-III	TRANSCEIVER ARCHITECTURES	Classes:10

General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

UNIT-IV	AMPLIFIERS, MIXERS AND OSCILLATORS	Classes:10

LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

UNIT-V	POWER AMPLIFIERS	Classes:10

General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques.

Text Books:

1. BehzadRazavi, RF Microelectronics Prentice Hall of India, 2001.
2. Thomas H. Lee, The Design of CMOS Radio Integrated Circuits, Cambridge University Press.

Reference Books:

1. G. Vendelin, “Design of Amplifiers and Oscillators by the S-Parameter Method”, John Wiley, 1982, ISBN 0-471-09226-6
2. T. Lee, “CMOS RFIC Design”, Cambridge University Press

Web References:

1.http://www.smdp2vlsi.gov.in/smdp2vlsi/downloads/RFICIEPSMDP2021stSept.pdf

2. https://en.wikipedia.org/wiki/Integrated_circuit_design

E-Text Books:

1. R. Williams, “Gallium Arsenide Processing Techniques” Artech House, 1984, ISBN 0-89006-152-1
2. B. Razavi, “RF Microelectronics” Prentice Hall, 1998, ISBN 0-13-887571-5

Outcomes:

1. Learn basic concepts of RF and wireless technology
2. Understand the various RF design concepts
3. Analyze techniques and wireless standards
4. Learn architecture of transreceiver
5. Study different types of power amplifiers, considerations and linearization techniques

MIXED SIGNAL LABORATORY

M.Tech II Semester – VLSI								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
		L	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
18VL209	Core	-	-	2	2	25	50	75
Contact Classes: Nil	**Tutorial Classes: Nil**	**Practical Classes: 39**			**Total Classes: 39**			

OBJECTIVES:

The course should enable the students to:

I. To teach students the fundamentals of analog/mixed-signal (analog & digital) circuit design

II. To teach students to use commercial design tools for schematic entry, simulation, and layout (the tools and process technology [Cadence] are close to the state of the art for analog design;

LIST OF EXPERIMENTS

Expt. 1	**ANALOG CIRCUITS SIMULATION USING SPICE**
This Experiment focus on simulation using SPICE	
Expt. 2	**MIXED SIGNAL SIMULATION USING MIXED SIGNAL SIMULATORS**
This Experiment focus on simulation using mixed signal simulator	
Expt. 3	**LAYOUT EXTRACTION FOR ANALOG & MIXED SIGNAL CIRCUITS**
This Experiment focus on layout extraction	
Expt. 4	**PARASITIC VALUES ESTIMATION FROM LAYOUT**
This Experiment focus on parasitic values estimation	
Expt. 5	**LAYOUT VS SCHEMATIC**
This Experiment focus on layout and schematic	
Expt. 6	**NET LIST EXTRACTION**
This Experiment focus on net list extraction	
Expt. 7	**DESIGN RULE CHECKS**
This Experiment focus on design rules	

Reference Books:

1. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill

Web References:

1. http://class.ece.iastate.edu/ee435/lectures/EE%20435%20Lect%201%20Spring%202014.pdf
2. https://www.ece.ucsb.edu/Faculty/rodwell/Classes/mixed_signal/mixed_signal.htm

Course Home Page:

SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 36 STUDENTS:

SOFTWARE: Xilinx 9.1i and Above for FPGA/CPLDS

HARDWARE: Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)

Course Outcome:

At the end of the course, a student will be able to:

1. Familiarize the Analog Circuits Simulation using Spice
2. Design of Layout Vs Schematic.
3. Generate Net List Extraction
4. Implements Design Rule Checks for various analog and digital designs

EMBEDDED PROCESSING LABORATORY

M.Tech II Semester – VLSI								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
		L	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
18VL210	Core	-	-	2	2	25	50	75
Contact Classes: Nil	**Tutorial Classes: Nil**	**Practical Classes: 39**			**Total Classes: 39**			

OBJECTIVES:

The course should enable the students to:

I. Discuss the major components that constitute an embedded system.
II. Implement small programs to solve well-defined problems on an embedded platform.
III. Develop familiarity with tools used to develop in an embedded environment.

LIST OF EXPERIMENTS

Expt. 1	**STUDY OF DIFFERENT ADDRESSING MODES USING 89C51/PIC MICROCONTROLLER**
To perform basic programming through addressing modes.	
Expt. 2	**GENERAL PURPOSE INPUT OUTPUT (GPIO) PORTS USING 89C51/PIC MICROCONTROLLER**
To configure GPIO port of 89C51.	
Expt. 3	**KEYBOARD INTERFACE USING EMBEDDED MICRO CONTROLLER**
To Interface Keyboard with embedded micro controller.	
Expt. 4	**LED AND LCD INTERFACE USING 89C50/PIC MICRO CONTROLLER**
To Interface LCD & LED with embedded micro controller.	
Expt. 5	**RTD AND THERMOCOUPLE INTERFACE USING EMBEDDED MICRO CONTROLLER**
To Interface RTD/ Thermocouple with embedded micro controller	
Expt. 6	**ADC AND DAC INTERFACE USING EMBEDDED MICRO CONTROLLER**
To Interface ADC & DAC with embedded micro controller	
Expt. 7	**I2C RTC INTERFACE USING EMBEDDED MICRO CONTROLLER**
To Interface I2C RTC with embedded micro controller	
Expt. 8	**ALARM CLOCK USING EMBEDDED MICRO CONTROLLER**
To Interface alarm clock with embedded micro controller	

Expt. 9	**TESTING RTOS ENVIRONMENT AND SYSTEM PROGRAMMING USING KEIL SOFTWARE**
To get familiar with RTOS environment using Keil.	
Expt. 10	**FLASH CONTROLLER PROGRAMMING - DATA FLASH WITH ERASE , VERIFY, FUSING THROUGH ATMEL/INTEL TOOLS**
To get familiar with Flash Programming	

Reference Books:

1. Muhammad Ali Mazidi, The 8050 Microcontroller and Embedded Systems: Using Assembly and C - VTU, Pearson, 2011

Web References:

1. https://en.wikipedia.org/wiki/Embedded_system
2. https://web.eecs.umich.edu/~jfr/embeddedctrls/files/embedded_controls_intro_W09.pdf

Course Home Page:

SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 36 STUDENTS:

SOFTWARE: Keil

HARDWARE: 8050, PIC and 89C50 Microcontroller Kit

Course Outcome:

At the end of the course, a student will be able to:

1. Familiarize with the ALP and C program using RTOS 8050 kits.
2. Dump the programs into the microcontroller kits using flash magic software.
3. Study ARM evaluation board and familiarize with basic programming concepts.
4. write programs to interface various I/O devices with PIC micro controllers

TERM PAPER

M.Tech II Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL211	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		0	0	4	2	50	-	50
Contact Classes: Nil	**Tutorial Classes: Nil**		**Practical Classes:20**			**Total Classes:20**		

The Term Paper is a self study report and shall be carried out either during II semester along with other lab courses. Every student will take up this term paper individually and submit a report. The scope of the term paper could be an exhaustive literature review choosing any engineering concept with reference to standard research papers or an extension of the concept of earlier course work in consultation with the term paper supervisor. The term paper reports submitted by the individual students during the II semester shall be evaluated for a total of 50 marks for continuous assessment; it shall be conducted by two Examiners, one of them being term paper supervisor as internal examiner and an external examiner nominated by the Principal from the panel of experts recommended by HOD.

HIGH SPEED VLSI
(Open Elective)

M.Tech III Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL301	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. Understand Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures

II. Design Non-Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families.

III. Know basic Latch design, Latching single-ended logic and Latching Differential Logic.

IV. Know Race Free Latch design, Signaling Standards, Chip-to-Chip Communication Networks.

V. Understand timing issues & clock generation.

UNIT-I	CLOCKED STRUCTURES	Classes:10

Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic

UNIT-II	NON-CLOCKED STRUCTURES	Classes:10

Non-Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families. Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise.

UNIT-III	DESIGN OF LATCH	Classes:10

Latching Strategies, Basic Latch Design, and Latching single-ended logic, Latching Differential Logic.

UNIT-IV	TECHNIQUES AND STANDARDS	Classes:10

Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques, Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection.

UNIT-V	CLOCKING GENERATION	Classes:10

Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques, Skew Tolerant Design

Text Books:

1. William S. Dally & John W. Poulton, “Digital Systems Engineering”, Cambridge University Press, 1998.
2. Kerry Bernstein &ET. Al., “High Speed CMOS Design Styles”, Kluwer, 1999.
3. Howard Johnson & Martin Graham, “High Speed Digital Design” A Handbook of Black Magic, Prentice Hall PTR, 1993.
4. Masakazu Shoji, “High Speed Digital Circuits”, Addison Wesley Publishing Company, 1996.
5. Jan M, Rabaey, et al, “Digital Integrated Circuits”, A Design Perspective, Pearson, 2003.

Reference Books:

1. Kerry Bernstein &et. al., “High Speed CMOS Design Styles”, Kluwer, 1999.
2. Evan Sutherland, Bob stroll, David Harris, “Logical Efforts, Designing Fast CMOS

Circuits", Kluwer, 1999.
3. David Harris, "Skew Tolerant Domino Design", Prentice Hall of India Private Ltd, 2000.

Web References:

1. https://ieeexplore.ieee.org/document/185018
2. https://www.tandfonline.com/doi/abs/10.1080/00207217.2018.1545256

E-Text Books:

1. Etienne Sicard, Sonia DelmasBendhia, "Basics of CMOS Cell Design", TMH, EEE, 2005.

Outcomes:

1. Gain knowledge on circuits and techniques involved in high speed VLSI circuits
2. Explore various design strategies to be followed for designing a high speed VLSI circuits.
3. Understand the logic styles for designing a high speed VLSI circuits

NANO ELECTRONICS
(Open Elective)

M.Tech III Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL302	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. To give an information for nanoelectronic systems and devices.

II. To provide the knowledge between these type of systems and quantum mechanical concepts.

UNIT-I	INTRODUCTION	Classes:10

Recent past, the present and its challenges, Future, Overview of basic Nano electronics.

UNIT-II	NANO ELECTRONICS & NANOCOMPUTER ARCHITECTURES	Classes:10

Introduction to Nanocomputers, Nanocomputer Architecture, Quantum DOT cellular Automata (QCA), QCA circuits, Single electron circuits, molecular circuits, Logic switches – Interface engineering, Properties (Self-organization, Size-dependent) – Limitations.

UNIT-III	NANOELECTRONIC ARCHITECTURES	Classes:10

Nanofabrication – Nanopatterning of Metallic/Semiconducting nanostructures (e-beam/X-ray, Optical lithography, STM/AFM- SEM & Soft-lithography) – Nano phase materials – Selfassembled Inorganic/Organic layers.

UNIT-IV	SPINTRONICS	Classes:10

Introduction, Overview, History & Background, Generation of Spin Polarization Theories of spin Injection, spin relaxation and spin dephasing, Spintronic devices and applications, spin filters, spin diodes, spin transistors.

UNIT-V	MEMORY DEVICES AND SENSORS	Classes:10

Memory devices and sensors – Nano ferroelectrics – Ferroelectric random access memory –Fe-RAM circuit design –ferroelectric thin film properties and integration – calorimetric -sensors – electrochemical cells – surface and bulk acoustic devices – gas sensitive FETs – resistive semiconductor gas sensors –electronic noses – identification of hazardous solvents and gases – semiconductor sensor array

Text Books:

1. Nanoelectronics&Nanosystems: From Transistor to Molecular & Quantum Devices: Karl Goser, JanDienstuhl and others.
2. Nano Electronics and Information Technology: Rainer Waser

Reference Books:

1. Nano Terchnology and Nano Electronics – Materials, devices and measurement Techniques by WR Fahrner – Springe
2. Nano: The Essentials – Understanding Nano Scinece and Nanotechnology by T.Pradeep;
   Tata Mc.Graw Hill.

Web References:

1. https://en.wikipedia.org/wiki/Nanoelectronics
2. https://onlinelibrary.wiley.com/doi/book/10.1002/9783527800728

E-Text Books:

1. James R Sheats and Bruce w.Smith, "Microlithography Science and Technology", Marcel Dekker Inc., New York, 1998.
2. J.P. Hirth and G.M.Pound "Evaporation: Nucleation and Growth Kinetics" Pergamon Press, Oxford, 1963

Outcomes:

1. Understand the divers electronic device fabrication.
2. Able to interact scientifically with industry both within and outside of a classroom setting.
3. Develop an appreciation of continuing educational and professional development.

AVAILABLE MOOCs
(Open Elective)

M.Tech III Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL303	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	0	0	4	40	60	100
Contact Classes:-	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:-**			

Meeting with the global requirements, to inculcate the habit of self learning and incompliance with UGC guidelines, MOOC (Massive Open Online Course) courses have been introduced as electives. The main intension to introduce MOOCs is to obtain enough exposure through online tutorials, self-learning at one's own pace, attempt quizzes, discuss with professors from various universities and finally to obtain certificate of completion for the course from the MOOCs providers

Regulations for MOOCs

- The respective departments shall give a list from NPTEL or any other standard providers, whose credentials are endorsed by the HOD.
- Each department shall appoint Coordinators/Mentors and allot the students to them who shall be responsible to guide students in selecting online courses and provide guidance for the registration, progress and completion of the same.
- A student shall choose an online course (relevant to his/her programme of study) from the given list of MOOCs providers, as endorsed by the teacher concerned, with the approval of the HOD.
- The details of MOOC(s) shall be displayed in Grade card of a student, provided he/she submits the proof of completion of it to the department concerned through the Coordinator/Mentor.
- Student can get certificate from SWAYAM/NPTEL or any other standard providers, whose credentials are endorsed by the HOD. The course work should not be less than 12 weeks or student may appear for end examination conducted by the Institute.
- There shall be one Mid Continuous Internal Examination (Quiz exam for 40 marks) after 9 weeks of the commencement of the course and semester end examination (Descriptive exam for 60 marks) shall be done along with the other regular courses.
- Three credits will be awarded upon successful completion of each MOOC courses having minimum of 8 weeks duration.

ADVANCED COMPUTER ARCHITECTURE
(Elective – V)

M.Tech III Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL304	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. Understand the micro-architectural design of processors

II. Learn about the various techniques used to obtain performance improvement and power savings in current processors

UNIT-I	FUNDAMENTALS OF COMPUTER DESIGN	Classes:10

Review of Fundamentals of CPU, Memory and IO – Trends in technology, power, energy and cost, Dependability – Performance Evaluation

UNIT-II	INSTRUCTION LEVEL PARALLELISM	Classes:10

ILP concepts – Pipelining overview – Compiler Techniques for Exposing ILP – Dynamic Branch Prediction – Dynamic Scheduling – Multiple instruction Issue – Hardware Based Speculation – Static scheduling – Multi-threading – Limitations of ILP – Case Studies.

UNIT-III	DATA-LEVEL PARALLELISM	Classes:10

Vector architecture – SIMD extensions – Graphics Processing units – Loop level parallelism.

UNIT-IV	THREAD LEVEL PARALLELISM	Classes:10

Symmetric and Distributed Shared Memory Architectures – Performance Issues – Synchronization – Models of Memory Consistency – Case studies: Intel i7 Processor, SMT & CMP Processors

UNIT-V	MEMORY AND I/O	Classes:10

Cache Performance – Reducing Cache Miss Penalty and Miss Rate – Reducing Hit Time – Main Memory and Performance – Memory Technology. Types of Storage Devices – Buses – RAID – Reliability, Availability and Dependability – I/O Performance Measures.

Text Books:

1. John L Hennessey and David A Patterson, “Computer Architecture A Quantitative Approach”, Morgan Kaufmann/ Elsevier, Fifth Edition, 2012.

Reference Books:

1. Kai Hwang and Faye Briggs, “Computer Architecture and Parallel Processing”, McGraw-Hill International Edition, 2000.
2. Sima D, Fountain T and Kacsuk P, ”Advanced Computer Architectures: A Design Space Approach”, Addison Wesley, 2000.

Web References:

1. https://onlinelibrary.wiley.com/doi/full/10.1002/9780470050118.ecse071
2. https://onlinelibrary.wiley.com/doi/pdf/10.1002/0471478385.fmatter

E-Text Books:

1. Rajiv Chopra, Advanced Computer Architecture, S. Chand Publishing, 2008

Outcomes:

1. Evaluate performance of different architectures with respect to various parameters
2. Analyze performance of different ILP techniques
3. Identify cache and memory related issues in multi-processors

SYSTEM ON CHIP ARCHITECTURE
(Elective – V)

M.Tech III Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL305	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. Design, optimize, and program a modern System-on-a-Chip.
II. Decompose the task into parallel components that cooperate to solve the problem.
III. Characterize and develop real-time solutions.
IV. Implement both hardware and software solutions, formulate hardware/software tradeoffs, and perform hardware/software codesign.
V. Understand the system on a chip from gates to application software, including on-chip memories and communication networks, I/O interfacing, RTL design of accelerators, processors, firmware and OS/infrastructure software.
VI. Understand and estimate key design metrics and requirements including area, latency, throughput, energy, power, predictability, and reliability.

UNIT-I	INTRODUCTION TO THE SYSTEM APPROACH	Classes:10

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II	PROCESSORS	Classes:10

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT-III	MEMORY DESIGN FOR SOC	Classes:10

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV	INTERCONNECT CUSTOMIZATION AND CONFIGURATION	Classes:10

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism

UNIT-V	APPLICATION STUDIES / CASE STUDIES	Classes:10

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Text Books:

1. Michael J. Flynn and Wayne Luk, Computer System Design System-on-Chip, Wiely India Pvt. Ltd.

2. Steve Furber, ARM System on Chip Architecture,2nd Ed., 2000, Addison Wesley Professional.

Reference Books:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

Web References:

1. https://en.wikipedia.org/wiki/System_on_a_chip
2. http://www.laccei.org/LACCEI2004-Miami/papers2/ET_024.doc

E-Text Books:

1. Prof Steve Furber, ARM System-on-Chip Architecture, Addison Wesley, 2000
2. Ahmed Jerraya and Wayne Wolf, Multiprocessor Systems-on-Chips, Elsevier, 2004

Outcomes:

1. Modeling and simulation of digital VLSI systems using hardware design language
2. To understand SOC architecture and instruction set.
3. Explain how design platforms can be used for an efficient design process
4. To understand soc interconnect architectures and understand bus structures.
5. Describe the design process for complex systems-on-chip
6. To analyze the soc system memory and cache memory.

FUNDAMENTALS AND APPLICATIONS OF MEMS
(Elective – V)

M.Tech III Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL306	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		4	-	-	4	40	60	100
Contact Classes:50	**Tutorial Classes: -**	**Practical Classes: Nil**			**Total Classes:50**			

OBJECTIVES:

The course should enable the students to :

I. To study the essential material properties
II. To study various sensing and transduction technique
III. To know about the polymer and optical MEMS

UNIT-I	INTRODUCTION TO MEMS	Classes:10

History of MEMS Development, Characteristics of MEMS-miniaturization - micro electronics integration -Mass fabrication with precision. Micro fabrication - microelectronics fabrication process- silicon based MEMS processes- new material and fabrication processing- points of consideration for processing.

UNIT-II	PROPERTIES OF MEMS	Classes:10

Conductivity of semiconductors, crystal plane and orientation, stress and stain – definition – relationship between tensile stress and stain- mechanical properties of silicon and thin films, Flexural beam bending analysis under single loading condition- Types of beam- deflection of beam-longitudinal stain under pure bendingspring constant, torsional deflection, intrinsic stress, resonance and quality factor.

UNIT-III	SENSING AND ACTUATION	Classes:10

Electrostatic sensing and actuation-parallel plate capacitor – Application-Inertial, pressure and tactile sensorparallel plate actuator- comb drive.

Thermal sensing and Actuations-thermal sensors-Actuators- Applications- Inertial, Flow and Infrared sensors.

Piezoresistive sensors- piezoresistive sensor material- stress in flexural cantilever and membraneApplication-Inertial, pressure, flow and tactile sensor. Piezoelectric sensing and actuation- piezoelectric material properties-quartz-PZT-PVDF –ZnOApplication-Inertial, Acoustic, tactile, flow-surface elastic waves

Magnetic actuation- Micro magnetic actuation principle- deposition of magnetic materials- Design and
fabrication of magnetic coil.

UNIT-IV	BULK AND SURFACE MICROMACHINING	Classes:10

Anisotropic wet etching, Dry etching of silicon, Deep reactive ion etching (DRIE), Isotropic wet
etching, Basic surface micromachining process- structural and sacrificial material, stiction and antistiction methods, Foundry process.

UNIT-V	POLYMER AND OPTICAL MEMS	Classes:10

Polymers in MEMS- polymide-SU-8 liquid crystal polymer(LCP)-PDMS-PMMA-Parylene-Flurocorbon, Application-Acceleration, pressure, flow and tactile sensors. Optical MEMS-passive MEMS optical components-lenses-mirrors-Actuation for active optical MEMS.

Text Books:

1. Chang Liu, “Foundations of MEMS”, Pearson International Edition, 2006.

Reference Books:

1. GaberielM.Rebiz, RF MEMS Theory,Design and Technology, John Wiley & Sons,2003
2. Charles P.Poole, Frank J.Owens, Introduction to nanotechnology, John Wiley & sons, 2003.
3. Julian W.Gardner, Vijay K Varadhan, Microsensors, MEMS and Smart devices, John Wiley and sons, 2001.

Web References:

1. https://www.lboro.ac.uk/microsites/mechman/research/ipm-ktn/pdf/Technology_review/an-introduction-to-mems.pdf
2. https://www.slideshare.net/navinec1/micro-electromechanical-system-mems

E-Text Books:

1. VikasChoudhary and Krzysztof Iniewski, MEMS: Fundamental Technology and Applications ARM System-on-Chip Architecture, CRC Press, 2017

Outcomes:

1. The student will have a broad knowledge in MEMS devices
2. The student will have a broad knowledge in Microfluidic structures
3. Student will be able to understand different fabrication and packaging techniques

PROJECT WORK PHASE – I

M.Tech III Semester: VLSI								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18VL307	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		0	0	20	10	Grade		
Contact Classes:-	**Tutorial Classes: -**	**Practical Classes: 40**				**Total Classes:40**		

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ concerned department.

- **Registration of Project work**: A candidate is permitted to register for the project work phase-I after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Semesters).
- An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor/ Guide and one Internal senior expert shall monitor the progress of the project work.
- The work on the project work phase-I shall be initiated in the III semester and continued in the final semester. The candidate can submit Project work phase-I dissertation with the approval of I.D.C. after 18 weeks from the date of registration at the earliest from the date of registration for the project work phase-I.
- The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.
- Three copies of the Dissertation certified in the prescribed form by the supervisor and HOD shall be submitted to the HOD.
- The semester end examination for project work phase-I done during III Semester, shall be conducted by a Project Review Committee (PRC). The evaluation of project work shall be conducted at the end of the III Semester.
- The PRC comprises of an External examiner appointed by the Principal, Head of the Department and Project Guide/Supervisor to adjudicate the dissertation. The PRC shall jointly evaluate candidates work and award grades as given below.

S.No	Description	Grade	Grade Point (GP) Assigned
1	Very Good	Grade A	10
2	Good	Grade B	9
3	Satisfactory	Grade C	8
4	Not satisfactory	Grade D	0

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the dissertation.

PROJECT WORK PHASE – II

M.Tech IVSemester: ELECTRICAL POWER SYSTEMS								
Course code	**Category**	**Hours/week**			**Credits**	**Maximum Marks**		
18EP401	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**TOTAL**
		0	0	32	16	Grade		
Contact Classes:-	**Tutorial Classes: -**	**Practical Classes: 60**				**Total Classes:60**		

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ concerned department.

- **Registration of Project work**: A candidate is permitted to register for the project work phase-I after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Semesters)
- An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor/ Guide and one Internal senior expert shall monitor the progress of the project work.
- The work on the project work phase-II shall be initiated in the IV semester. The candidate can submit Project work phase-II dissertation with the approval of I.D.C. after 18 weeks from the date of registration at the earliest from the date of registration for the project work phase-I.
- The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.
- Three copies of the Dissertation certified in the prescribed form by the supervisor and HOD shall be submitted to the HOD.
- The semester end examination for project work phase-I done during III Semester, shall be conducted by a Project Review Committee (PRC). The evaluation of project work shall be conducted at the end of the IV Semester.
- The PRC comprises of an External examiner appointed by the Principal, Head of the Department and Project Guide/Supervisor to adjudicate the dissertation. The PRC shall jointly evaluate candidates work and award grades as given below

S.No	Description	Grade	Grade Point (GP) Assigned
1	Very Good	Grade A	10
2	Good	Grade B	9
3	Satisfactory	Grade C	8
4	Not satisfactory	Grade D	0

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the dissertation.