# AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY

**(AUTONOMOUS)**

**(Approved by AICTE | Accredited by NAAC | Affiliated to JNTUA)**

**Gudur, Nellore Dist - 524101, A.P (India)**

# OUTCOME BASED EDUCATION

# WITH

# CHOICE BASED CREDIT SYSTEM

## MASTER OF TECHNOLOGY

## EMBEDDED SYSTEMS

## ACADEMIC REGULATIONS

## UNDER AUTONOMOUS STATUS

**M.Tech Regular Two Year PG Programme**

**(for the batches admitted from the academic year 2018 - 2019)**

## ACADEMIC REGULATIONS (R18) FOR M.TECH. REGULAR STUDENTS WITH EFFECT FROM ACADEMIC YEAR 2018-2019

1.0 Post- Graduate Degree Programme in Engineering & Technology

1.1 These academic rules and regulations are applicable to the students admitted from the academic year 2018-19 onwards into 2 year (4 Semesters) M.Tech Programmes under Choice Based Credit System( CBCS) at its autonomous institution with effect from the academic year 2018-19 in the following specializations of Engineering:

### M.Tech Specializations offered

1. Embedded Systems (ES)
2. VLSI (VL)
3. Electrical Power Systems (EP)
4. Power Electronics (PE)
5. Computer Science & Engineering (CO)
6. Software Engineering (SE)
7. Structural Engineering (ST)

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| **2.0** | **Eligibility for admission** |
| **2.1** | Admission to the post graduate programme shall be made either on the basis of the merit rank obtained by the qualified student in entrance test PGECET conducted by the Andhra Pradesh State Government as per the norms of Andhra Pradesh State Council of Higher Education (APSCHE) |
| **2.2** | The medium of instructions for the entire post graduate programme in Engineering & Technology will be English only. |
| **3.0** | **M.Tech. Programme Pattern** |
| **3.1** | A student after securing admission shall pursue the post graduate programme in M.Tech in a minimum period of two academic years (4 semesters), and a maximum period of four academic years (8 semesters) starting from the date of commencement of first year first semester, failing which student shall forfeit the M.Tech course. Each semester is structured to around 20 credits, totaling to 78 credits for the entire M.Tech programme. Each student shall secure 78 credits required for the completion of the post graduate programme and award of the M.Tech degree. |
| **3.2** | A student eligible to appear for the end examination in a course, but absent or has failed in the end examination may appear for that course at the next supplementary examination when offered |

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| **3.3** | When a student is detained due to lack of shortage of attendance he/she may be re-admitted when the semester is offered after fulfillment of academic regulations. In such case, he/she shall be in the academic regulations into which he/she is readmitted. |
| **3.4** | UGC/ AICTE specified definitions/ descriptions are adopted appropriately for various terms and abbreviations used in these academic regulations/ norms, which are listed below. |
| **3.5** | **Semester scheme**<br>Each under graduate programme is of 2 academic years (4 semesters) with the academic year being divided into two semesters of 16 weeks (around 90 instructional days) each and semester having – Continuous Internal Evaluation (CIE) and Semester End Examination (SEE). Choice based Credit System (CBCS) and Credit Based Semester System (CBSS) as indicated by UGC and curriculum / course structure as suggested by AICTE are followed. |
| **3.6** | **Credit courses**<br>All subjects/ courses are to be registered by the student in a semester to earn credits which shall be assigned to each subject/ course in an L: T: P: C (lecture periods: Tutorial periods: Practical periods: Credits) structure based on the following general pattern.<br>• One credit for one hour/ week/ semester for theory/ lecture (L) courses.<br>• One credit for two hours/ week/ semester for laboratory/ practical (P) courses or Tutorials (T). |
| **3.7** | **Subject Course Classification**<br>All subjects/ courses offered for the post graduate programme in Engineering & Technology (M.Tech. degree programmes) are broadly classified as follows. The ASCET has followed almost all the guidelines issued by AICTE/UGC. |
| **4.0** | **Attendance requirements:** |
| **4.1** | A student shall be eligible to appear for the semester end examinations, if student acquires a minimum of 75% of attendance in aggregate of all the subjects/ courses for that semester. |
| **4.2** | Shortage of attendance in aggregate up to 10% (65% and above, and below 75%) in each semester may be condoned by the college academic committee on genuine and valid grounds, based on the student's representation with supporting evidence. |
| **4.3** | A stipulated fee shall be payable towards condonation for shortage of attendance to the institute as decided by the College Academic Committee. |
| **4.4** | Shortage of attendance below 65% in aggregate shall in no case be condoned. |
| **4.5** | Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examinations of that semester. They get detained and their registration for that semester shall stand cancelled. They will not be promoted to the next semester. They may seek re-registration for all those subjects registered in that semester in which student was detained, by seeking re-admission into that semester as and when offered; in case if there are any professional electives and/ or open electives, the same may also be re-registered if offered. However, if those electives are not offered in later semesters, then alternate electives may be chosen from the same set of elective subjects offered under that category. |

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| **4.6** | A student fulfilling the attendance requirement in the present semester shall not be eligible for readmission into the same class. |
| **5.0** | **Academic requirements**<br>The following academic requirements have to be satisfied, in addition to the attendance requirements mentioned in item no.4. |
| **5.1** | A student shall be deemed to have satisfied the minimum academic requirements and earned the credits allotted to each theory, practical, design, drawing subject or project if he secures not less than 40% of marks (i.e., 24) in the end semester examination and a minimum of 50% of marks (i.e., 50) in the sum total of the internal evaluation and end examination taken together. |
| **5.6** | A student shall register and put up minimum attendance in all 78 credits and earn all the 78 credits. Marks obtained in all 78 credits shall be considered for the calculation of aggregate percentage of marks obtained |
| **5.7** | Students who fail to earn 78 credits as indicated in the course structure within eight academic years from the year of their admission shall forfeit their seat in M.Tech. Course and their admission shall stand cancelled |
| **6.0** | **Distribution and Weightage of marks** |
| **6.1** | The performance of a student in each semester shall be evaluated through internal evaluation and /or an external evaluation conducted semester wise. |
| **6.2** | The performance of a student in every theory course shall be evaluated for total of 100 marks each, of which the relative weightage for Continuous Internal Evaluation and Semester End Examination shall be 40 marks and 60 marks respectively. |
| **6.3** | The performance of a student in every practical course shall be evaluated for total of 75 marks each, of which the relative weightage for Continuous Internal Evaluation and Semester End Examination shall be 25 marks and 50 marks respectively. |
| **6.4** | **Internal Evaluation for Theory Course:**<br>The total internal weightage for theory courses is 40 marks with the following distribution.<br>➢ 30 marks for Mid-Term Examination<br>➢ 10 marks for Assignment Test<br>While the first mid-term examination shall be conducted on the 50% of the syllabus (Unit-I, Unit-II, & 50% of Unit-III), the second mid-term examination shall be conducted on the remaining 50% of the syllabus (50 % of Unit III, Unit-IV & Unit-V).<br>10 marks are allocated for assignment test (as specified by the subject teacher concerned). The first assignment should be conducted after completion of Unit-I for 5 marks and the second assignment should be conducted after completion of Unit- IV for 5 marks. The final Assignment Test marks will be the addition of these two.<br>Two midterm examinations each for **30 marks** with the duration of 90 minutes each will be conducted for every theory course in a semester. The midterm examination marks shall be awarded giving a weightage of 80% in the midterm examination in which the student scores |

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| | better performance and 20% in the remaining midterm examination.<br>The final mid-term marks obtain by the addition of these two (80% + 20%).<br>**Example**: If a student scores 33 marks and 34 marks in the first and second mid-term examinations respectively, then Weighted Average Marks = 34 x 0.8 + 33 x 0.2 = 33.8, rounded to 34 Marks.<br>**Note**: The marks of any fraction shall be rounded off to the next higher mark. |
| **6.5** | **Pattern of the midterm examination question paper is as follows:**<br>➢ A total of three questions<br>➢ Question paper contains six questions are to be designed taking three questions from each unit (Unit Wise - Either or type) of the three units. (3X10=30 Marks)<br>**Pattern of the Assignment Test is as follows:**<br>➢ Five assignment questions are given in advance, out of which two questions given by the concerned teacher has to be answered during the assignment test<br>➢ Sum of Assignment Tests marks is considered.<br>**Note:** A student who is absent for any Mid-Term Examination/ Assignment Test, for any reason whatsoever, shall be deemed to have scored zero marks in that Mid-Term Examination/ Assignment Test and no make-up test shall be conducted. |
| **6.6** | **Internal Evaluation for Practical Course:**<br>For practical subjects there shall be a Continuous Internal Evaluation during the semester for 25 internal marks. Out of the 25 marks for internal evaluation, day-today assessment in the laboratory shall be evaluated for 10 marks and internal practical examination shall be evaluated for 15 marks conducted by the laboratory teacher concerned. |
| **6.7** | **Internal Evaluation for Term Paper:**<br>The Term Paper is a self study report and shall be carried out either during II semester along with other lab courses. Every student will take up this term paper individually and submit a report. The scope of the term paper could be an exhaustive literature review choosing any engineering concept with reference to standard research papers or an extension of the concept of earlier course work in consultation with the term paper supervisor. The term paper reports submitted by the individual students during the II semester shall be evaluated for a total of 50 marks for continuous assessment; it shall be conducted by two Examiners, one of them being term paper supervisor as internal examiner and an external examiner nominated by the Principal from the panel of experts recommended by HOD. |
| **6.8** | **Project Work:**<br>The Project work is spread over to two semesters having Project Work Phase-I and Project Work Phase-II. Project Work Phase-I is included in III Semester and Project Work Phase-II in IV Semester as detailed below:<br>A student has to select topic of his Project Work based on his interest and available facilities, in the III semester which he will continue through IV semester also. |
| **6.9** | **External Evaluation for Theory Course - Semester End Examination:**<br>The Semester End Examination in each theory subject shall be conducted for 3 hours duration |

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| | at the end of the semester for 60 marks.<br>**Pattern of the Semester End Examination question paper is as follows:**<br>➢ Question Paper contains ten questions are to be designed taking two questions from each unit (Unit Wise - Either or type) of the total five units. (5X12=60 Marks)<br>A student has to secure not less than a minimum of 40% of marks (24 marks) exclusively at the Semester End Examinations in each of the theory subjects in which the candidate had appeared. However, the candidate shall have to secure a minimum of 50% of marks (50 marks) in both external and internal components put together to become eligible for passing in the subject. |
| **6.10** | **External Evaluation for Practical Course**<br>Out of 50 marks **35** marks are allocated for experiment (procedure for conducting the experiment carries 15 marks & readings, calculation and result-20) and **10** marks for viva-voce examination with **5** marks for the record.<br>Each Semester External Lab Examination shall be evaluated by an Internal Examiner along with an External Examiner appointed by the Principal.<br>A candidate shall be declared to have passed in individual lab course if he secures a minimum of 50% aggregate marks (38 marks) (Internal & Semester External Examination marks put together), subject to a minimum of 50% marks (25 marks) in the semester external examination. |
| **6.11** | **Project Work Phase-I:**<br>Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ concerned department.<br>➢ **Registration of Project work**: A candidate is permitted to register for the project work phase-I after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Semesters).<br>➢ An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor/ Guide and one Internal senior expert shall monitor the progress of the project work.<br>➢ The work on the project work phase-I shall be initiated in the III semester and continued in the final semester. The candidate can submit Project work phase-I dissertation with the approval of I.D.C. after 18 weeks from the date of registration at the earliest from the date of registration for the project work phase-I.<br>• The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.<br>• Three copies of the Dissertation certified in the prescribed form by the supervisor and HOD shall be submitted to the HOD.<br>• The semester end examination for project work phase-I done during III Semester, shall be conducted by a Project Review Committee (PRC). The evaluation of project work shall be conducted at the end of the III Semester. |

- The PRC comprises of an External examiner appointed by the Principal, Head of the Department and Project Guide/Supervisor to adjudicate the dissertation. The PRC shall jointly evaluate candidates work and award grades as given below.

| S.No | Description | Grade | Grade Point (GP) Assigned |
|---|---|---|---|
| 1 | Very Good | Grade A | 10 |
| 2 | Good | Grade B | 9 |
| 3 | Satisfactory | Grade C | 8 |
| 4 | Not satisfactory | Grade D | 0 |

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the dissertation.

**6.12 Project Work Phase-II:**

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ concerned department.

- **Registration of Project work**: A candidate is permitted to register for the project work phase-I after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Semesters)
- An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor/ Guide and one Internal senior expert shall monitor the progress of the project work.
- The work on the project work phase-II shall be initiated in the IV semester. The candidate can submit Project work phase-II dissertation with the approval of I.D.C. after 18 weeks from the date of registration at the earliest from the date of registration for the project work phase-I.

- The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.
- Three copies of the Dissertation certified in the prescribed form by the supervisor and HOD shall be submitted to the HOD.
- The semester end examination for project work phase-I done during III Semester, shall be conducted by a Project Review Committee (PRC). The evaluation of project work shall be conducted at the end of the IV Semester.
- The PRC comprises of an External examiner appointed by the Principal, Head of the Department and Project Guide/Supervisor to adjudicate the dissertation. The PRC shall jointly evaluate candidates work and award grades as given below

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If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the dissertation.

**6.13** **Re-Registration For Improvement of Internal Evaluation Marks:**

Following are the conditions to avail the benefit of improvement of internal evaluation marks.

- The candidate should have completed the course work and obtained examinations results for I, II & III semesters.
- He should have passed all the subjects for which the internal evaluation marks secured are more than 50%.
- Out of the subjects the candidate has failed in the examination due to Internal evaluation marks secured being less than 50%, the candidate shall be given one more chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.
- The candidate has to re-register for the subjects so chosen and fulfill all the academic requirements.
- For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of **'The Principal, Audisankara College of Engineering & Technology' payable at Gudur** along with the requisition through the Controller of the Examinations of the college.
- In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

**7.0** **SEMESTER – WISE DISTRIBUTION OF CREDITS**

| Semester | Theory | Practicals | Credits |
|---|---|---|---|
| M.Tech I Semester | 5 | 2 | 22 |
| M.Tech II Semester | 4 | 2 + Term Paper | 22 |
| M.Tech III Semester | 2 | Project Work Phase-I | 18 |
| M.Tech IV Semester | 0 | Project Work Phase-II | 16 |
| | | Total | 78 |

**8.0 GRADING PROCEDURE**

Grades will be awarded to indicate the performance of students in each theory subject, laboratory / practicals, Term Paper and project Work Phase-I & II. Based on the percentage of marks obtained (Continuous Internal Evaluation plus Semester End Examination, both taken together) as specified in item 6 above, a corresponding letter grade shall be given.

**8.1** As a measure of the performance of a student, a 10-point absolute grading system using the following letter grades (as per UGC/AICTE guidelines) and corresponding percentage of marks shall be followed:

| Marks Range | Letter Grade | Grade Points |
|---|---|---|
| 91-100 | S (Superior) | 10 |
| 81-90 | A (Excellent) | 9 |
| 70-80 | B (Very Good) | 8 |
| 60-69 | C (Good) | 7 |
| 55-59 | D (Average) | 6 |
| 50-54 | E (Pass) | 5 |
| <50 | F (FAIL) | 0 |
| Ab (Absent) | Ab | 0 |

**8.2** A student who has obtained an 'F' grade in any subject shall be deemed to have 'failed' and is required to reappear as a 'supplementary student' in the semester end examination, as and when offered. In such cases, internal marks in those subjects will remain the same as those obtained earlier

**8.3** To a student who has not appeared for an examination in any subject, 'Ab' grade will be allocated in that subject, and he is deemed to have 'failed'. A student will be required to reappear as a 'supplementary student' in the semester end examination, as and when offered next. In this case also, the internal marks in those subjects will remain the same as those obtained earlier.

**8.4** A letter grade does not indicate any specific percentage of marks secured by the student, but it indicates only the range of percentage of marks.

**8.5** A student earns grade point (GP) in each subject/ course, on the basis of the letter grade secured in that subject/ course. The corresponding 'credit points' (CP) are computed by multiplying the grade point with credits for that particular subject/ course.

Credit points (CP) = grade point (GP) x credits …. For a course

**8.6** A student passes the subject/ course only when GP ≥5 ('E' grade or above)

**8.7**

- A student obtaining Grade F shall be considered failed and will be required to reappear for that subject when the next supplementary examination offered.
- For Mandatory courses "Satisfactory" or "Unsatisfactory" shall be indicated instead

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| | of the letter grade and this will not be counted for the computation of SGPA/CGPA. |
| **8.8** | **Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):**<br>The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.<br>$$SGPA = \sum_{i=1}^{n}(Ci \times Gi)/\sum_{i=1}^{n} Ci$$<br>Where, Ci is the number of credits of the $i^{th}$ subject, Gi is the grade point scored by the student in the $i^{th}$ course and n is the number of subjects.<br>The Cumulative Grade Point Average (CGPA) will be computed in the same manner taking into account all the courses undergone by a student over all the semesters of a program, i.e.<br>$$CGPA = \sum_{i=1}^{n}(Ci \times Si)/\sum_{i=1}^{n} Ci$$<br>Where 'Si' is the SGPA of the $i^{th}$ semester, Ci is the total number of credits in that semester and n is the number of semesters.<br>Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.<br>While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included.<br>***Grade Point:*** It is a numerical weight allotted to each letter grade on a 10-point scale.<br>***Letter Grade:*** It is an index of the performance of students in a said course. Grades are denoted by letters as mentioned in the above table. |
| **9.0** | **Award of Class** |
| **9.1** | After a student has satisfied the requirement prescribed for the completion of the program and is eligible for the award of M.Tech. Degree he/she shall be placed in one of the following four classes: |

| Class Awarded | CGPA Secured |
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| First class with Distinction | >= 8 |
| First class | >= 7 and < 8 |
| Second class | >= 5 and < 7 |

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| **10.0** | **Transitory regulations** |
| **10.1** | For students detained due to shortage of attendance:<br>1. A Student who has been detained in I year of R16 Regulations due to lack of |

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| | attendance, shall be permitted to join I year I Semester of R18 Regulations and he is required to complete the study of M.Tech/ programme with in the stipulated period of eight academic years from the date of first admission in I year.<br>2. A student who has been detained in any semester of II, III and IV years of R16 regulations for want of attendance, shall be permitted to join the corresponding semester of R18 regulations and is required to complete the study of M.Tech within the stipulated period of eight academic years from the date of first admission in I Year. The R18 Academic Regulations under which a student has been readmitted shall be see rule 10.3 for further Transitory Regulations. |
| **10.2** | For students detained due to shortage of credits:<br>A student of R16 Regulations who has been detained due to lack of credits, shall be promoted to the next semester of R18 Regulations only after acquiring the required credits as per the corresponding regulations of his/her first admission. The student is required to complete the study of M.Tech. within the stipulated period of eight academic years from the year of first admission. The R18 Academic Regulations are applicable to a student from the year of readmission onwards. See rule 10.3 for further Transitory Regulations. |
| **10.3** | For readmitted students in R18 Regulations:<br>1. A student who has failed in any subject under any regulation has to pass those subjects in the same regulations.<br>2. The maximum credits that a student acquires for the award of degree, shall be the sum of the total number of credits secured in all the regulations of his/her study including R18 Regulations.<br>3. If a student readmitted to R18 Regulations, has any subject with 80% of syllabus common with his/her previous regulations, that particular subject in R18 Regulations will be substituted by another subject to be suggested by the College standing committee.<br>Note: If a student readmitted to R18 Regulations, has not studied any subjects/topics in his/her earlier regulations of study which is prerequisite for further subjects in R18 Regulations, the department HOD concerned shall conduct remedial classes to cover those subjects/topics for the benefit of the students. |
| **11.0** | **Supplementary Examinations:**<br>Apart from the regular End Examinations the institute may also schedule and conduct supplementary examinations for all subjects for the benefit of students with backlogs. Such students writing supplementary examinations as supplementary candidates may have to write more than one examination per day. |
| **12.0** | **Student Transfers**<br>Student transfers shall be as per the guidelines issued by the Government of Andhra Pradesh from time to time. |

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| **13.0** | **With–Holding of Results**<br>If the candidate has any dues not paid to the institute or if any case of indiscipline or malpractice is pending against him/her, the result of the candidate shall be withheld and he/she will not be allowed / promoted into the next higher semester. The issue of awarding degree is liable to be withheld in such cases. |
| **12.0** | **Conduct and Discipline**<br>➢ Students shall conduct themselves within and outside the premises of the Institute in a descent and dignified manner befitting the students of Audisankara College of Engineering & Technology.<br>➢ As per the order of the Honorable Supreme Court of India, ragging in any form is considered a criminal offence and is totally banned. Any form of ragging will be severely dealt with<br>The following acts of omission and / or commission shall constitute gross violation of the code of conduct and are liable to invoke disciplinary measures with regard to ragging.<br>(i) Lack of courtesy and decorum; indecent behavior anywhere within or outside the college campus.<br>(ii) Damage of college property or distribution of alcoholic drinks or any kind of narcotics to fellow students / citizens.<br>➢ Possession, consumption or distribution of alcoholic drinks or any kind of narcotics or hallucinogenic drugs.<br>➢ Mutilation or unauthorized possession of library books.<br>➢ Noisy and unruly behavior, disturbing studies of fellow students.<br>➢ Hacking in computer systems (such as entering into other person's areas without prior permission, manipulation and / or damage of computer hardware and software or any other cyber crime etc.<br>➢ Usage of camera /cell phones in the campus.<br>➢ Plagiarism of any nature.<br>➢ Any other act of gross indiscipline as decided by the college academic council from time to time.<br>➢ Commensurate with the gravity of offense, the punishment may be reprimand, fine, expulsion from the institute/ hostel, debarring from examination, disallowing the use of certain facilities of the Institute, rustication for a specified period or even outright expulsion from the Institute, or even handing over the case to appropriate law enforcement authorities or the judiciary, as required by the circumstances.<br>➢ For an offence committed in (i) a hostel (ii) a department or in a class room and (iii) elsewhere, the chief Warden, the concern Head of the Department and the Principal respectively, shall have the authority to reprimand or impose fine.<br>➢ Cases of adoption of unfair means and/ or any malpractice in an examination shall be |

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| | reported to the principal for taking appropriate corrective action.<br>➢ All cases of serious offence, possibly requiring punishment other than reprimand, shall be reported to the Academic council of the college.<br>➢ The Institute Level Standing Disciplinary Action Committee constituted by the academic council shall be the authority to investigate the details of the offence, and recommend disciplinary action based on the nature and extent of the offence committed.<br>➢ The Principal shall deal with any problem, which is not covered under these rules and regulations.<br>➢ **"Grievance and Redressal Committee" (General)** constituted by the Principal shall deal with all grievances pertaining to the academic / administrative / disciplinary matters.<br>➢ All the students must abide by the code and conduct rules prescribed by the college from time to time. |
| **13.0** | **General**<br>➢ s/he represents "she" and "he" both<br>➢ Where the words 'he', 'him', 'his', occur, they imply 'she', 'her', 'hers' also.<br>➢ The academic regulations should be read as a whole for the purpose of any interpretation.<br>➢ In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman, Academic Council will be final.<br>The college may change or amend the academic regulations or syllabi from time to time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the institute. |

**RULES FOR**
**DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS**

| | Nature of Malpractices/Improper conduct | Punishment |
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| 1. (a) | Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers, blue tooth or any other form of material concerned with or related to the course of the examination (theory or practical) in which he/she is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the course of the examination) | Expulsion from the examination hall and cancellation of the performance in that course only. |
| (b) | Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the examination hall in respect of any matter. | Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he/she will be handed over to the police and a case is registered against him. |
| 2 | Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the course of the examination (theory or practical) in which the candidate is appearing. | Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that Semester/year. The Hall Ticket of the candidate is to be cancelled. |
| 3 | Impersonates any other candidate in connection with the examination | The candidate who has impersonated shall be expelled from examination hall. The Candidate is also debarred for four consecutive semesters from class work and all end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with for |

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| | | feature of seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the courses of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that Semester/year. The candidate is also debarred for four consecutive Semesters from class work and all Semester end examinations if his involvement is established. Otherwise the candidate is debarred for two consecutive semesters from class work and all end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he/she will be handed over to the police and a case is registered against him. |
| 4 | Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination. | Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that Semester/year. The candidate is also debarred for two consecutive Semesters from class work and all Semester end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. |
| 5 | Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks. | Cancellation of the performance in that course. |
| 6 | Refuses to obey the orders of the any officer on duty or misbehaves or creates disturbance of any kind in and around the | In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that |

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| | examination hall or organizes a walkout or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination. | course and all other courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the courses of that Semester. If candidate physically assaults the invigilator or/officer in charge of the examination, then the candidate is also barred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them. |
| 7 | Leaves the examination hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall. | Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that Semester/year. The candidate is also debarred for two consecutive Semesters from class work and all Semester end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. |
| 8 | Possess any lethal weapon or firearm in the examination hall | Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that |

| | | |
|---|---|---|
| | | Semester/year. The candidate is also debarred and forfeits the seat. |
| 9 | If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8. | Student of the colleges expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the Courses of that Semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them. |
| 10 | Comes in a drunken condition to the examination hall. | Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that Semester/year. |
| 11 | Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny. | Cancellation of the performance in that course and all other courses the candidate has appeared including practical examinations and project work of that Semester examinations depending on the recommendation of the committee. |
| 12 | If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Principal for further action to award suitable punishment. | |

**Note:**

i. All malpractices cases are to be handled by the Chief Controller with a committee consist of Controller of Examinations, HOD concerned and subject expert.

ii. Whenever the performance of a student is cancelled in any course/ courses due to Malpractice, he has to register for the End Examination in those course/courses consequently and has to fulfill all the norms required for award of Degree.

## COURSE STRUCTURE

**M.Tech I Semester – Embedded Systems**

| S.No | Course Code | Course Title | Hours per Week | | | Marks | | | Credits |
|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | IM | EM | T | |
| 1 | 18ES101 | Microcontrollers for Embedded System Design | 4 | 0 | 0 | 40 | 60 | 100 | 4 |
| 2 | 18ES102 | Embedded System Concepts | 4 | 0 | 0 | 40 | 60 | 100 | 4 |
| 3 | **Elective-I** | | | | | | | | |
| | 18ES103 | VLSI Technology and Design | 4 | 0 | 0 | 40 | 60 | 100 | 4 |
| | 18ES104 | Embedded Computing | | | | | | | |
| | 18ES105 | Advanced Operating Systems | | | | | | | |
| 4 | **Elective-II** | | | | | | | | |
| | 18ES106 | DSP Processors and Architectures | 4 | 0 | 0 | 40 | 60 | 100 | 4 |
| | 18ES107 | CMOS Digital Integrated Circuit Design | | | | | | | |
| | 18ES108 | Embedded C | | | | | | | |
| 5 | 18AS101 | Research Methodology and IPR | 2 | 0 | 0 | 40 | 60 | 100 | 2 |
| 6 | 18ES110 | Microcontrollers and Interfacing Lab | 0 | 0 | 4 | 25 | 50 | 75 | 2 |
| 7 | 18ES111 | VLSI Design Lab | 0 | 0 | 4 | 25 | 50 | 75 | 2 |
| | | **Total** | **18** | **0** | **8** | **250** | **400** | **650** | **22** |

**M.Tech II Semester – Embedded Systems**

| S.No | Course Code | Course Title | Hours per Week | | | Marks | | | Credits |
|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | IM | EM | T | |
| 1 | 18ES201 | FPGA Architecture and Applications | 4 | 0 | 0 | 40 | 60 | 100 | 4 |
| 2 | 18ES202 | Real Time Operating Systems | 4 | 0 | 0 | 40 | 60 | 100 | 4 |
| 3 | **Elective-III** | | | | | | | | |
| | 18ES203 | System on Chip Architecture | 4 | 0 | 0 | 40 | 60 | 100 | 4 |
| | 18ES204 | Cryptography and Network Security | | | | | | | |
| | 18ES205 | Embedded Networks | | | | | | | |
| 4 | **Elective-IV** | | | | | | | | |
| | 18ES206 | Hardware Software Co-Design | 4 | 0 | 0 | 40 | 60 | 100 | 4 |
| | 18ES207 | TCP / IP Internetworking | | | | | | | |
| | 18ES208 | Software Defines Radio | | | | | | | |
| 5 | 18ES209 | RTOS and FPGA Lab | 2 | 0 | 0 | 40 | 60 | 100 | 2 |
| 6 | 18ES210 | Advanced Embedded Systems Lab | 0 | 0 | 4 | 25 | 50 | 75 | 2 |
| 7 | 18ES211 | Term Paper | 0 | 0 | 4 | 50 | - | 50 | 2 |
| | | **Total** | **18** | **0** | **8** | **275** | **350** | **625** | **22** |

**M.Tech III Semester – Embedded Systems**

| S.No | Course Code | Course Title | Hours per Week | | | Marks | | | Credits |
|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | IM | EM | T | |
| 1 | | **Open Elective** | 4 | 0 | 0 | 40 | 60 | 100 | 4 |
| 2 | **Elective-V** | | | | | | | | |
| | 18ES304 | Advanced Computer Architecture | 4 | 0 | 0 | 40 | 60 | 100 | 4 |
| | 18ES305 | Robotic Technology | | | | | | | |
| | 18ES306 | Embedded Wireless Sensor Networks | | | | | | | |
| 3 | 18ES307 | Project Work Phase-I | 0 | 0 | 20 | Grade | | | 10 |
| **Total** | | | **8** | **0** | **8** | **80** | **120** | **200** | **18** |

**M.Tech IV Semester – Embedded Systems**

| S.No | Course Code | Course Title | Hours per Week | | | Marks | | | Credits |
|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | IM | EM | T | |
| 1 | 18ES401 | Project Work Phase-II | 0 | 0 | 32 | Grade | | | 16 |
| **Total** | | | **0** | **0** | **32** | **Grade** | | | **16** |

**Open Electives – Embedded Systems**

| S.No | Course Code | Course Title |
|---|---|---|
| 1 | 18ES301 | Embedded Linux |
| 2 | 18ES302 | Fundamentals and Applications Of MEMS |
| 3 | 18ES303 | Available MOOCs |

# MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

| **M.Tech I Semester: EMBEDDED SYSTEM** | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES101** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to:**

I. To have knowledge about the basic working of a microcontroller system and its programming in assembly language.

II. To provide experience to integrate hardware and software for microcontroller applications systems

| **UNIT-I** | **ARM ARCHITECTURE** | **Classes:10** |
|---|---|---|

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families

| **UNIT-II** | **ARM PROGRAMMING MODEL – I** | **Classes:10** |
|---|---|---|

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

| **UNIT-III** | **ARM PROGRAMMING MODEL – II** | **Classes:10** |
|---|---|---|

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

| **UNIT-IV** | **ARM PROGRAMMING** | **Classes:10** |
|---|---|---|

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

| **UNIT-V** | **MEMORY MANAGEMENT** | **Classes:10** |
|---|---|---|

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

**Text Books:**

1. Andrew N. Sloss, Dominic Symes, Chris Wright, ARM Systems Developer's Guides-Designing & Optimizing System Software, Elsevier, 2008.

**Reference Books:**

1. Jonathan W. Valvano – Brookes / Cole, Embedded Microcomputer Systems, Real Time Interfacing,Thomas Learning, 1999.

**Web References:**

1. https://en.wikipedia.org/wiki/Embedded_system
2. https://www.springer.com/in/book/9781402083921

**E-Text Books:**

1. Embedded systems design by Steve Heath, Newnes.
2. The 8050 Microcontroller and embedded systems by Muhammad Ali Mazidi, PHI.
3. PIC microcontroller and embedded systems by Muhammad Ali Mazidi, PHI.

**Outcomes:**

1. To understand outline architecture of ARM7 microcontroller including basics of pipelines, registers, exception modes, etc.
2. To learn ARM7 instruction set covering branching, data processing instructions, swap instruction, THUMB instruction set and others.
3. To learn Software development flow and working with projects.
4. To give an overview of system peripherals which cover bus structure, memory map, register programming.
5. To set up and customize a microcontroller development environment.
6. To understand the basic concepts of memory management in ARM microcontroller

# EMBEDDED SYSTEM CONCEPTS

| M.Tech I Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES102** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To introduce students to the modern embedded systems and to show how to understand and program such systems using a concrete platform built around

II. A modern embedded processor like the Intel ATOM.

| UNIT-I | INTRODUCTION | Classes:10 |
|---|---|---|

**Introduction to Embedded Systems:** An Embedded System, Processor in The System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System -On-Chip (SOC) and in VLSI Circuit.

**Processor and Memory Organization:** Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

| UNIT-II | DEVICES AND BUSES FOR DEVICE NETWORKS | Classes:10 |
|---|---|---|

I/O Devices, Timer and Counting Devices, Serial Communication Using The "$I^2C$" , CAN, Profibus Foundation Field Bus. and Advanced I/O Buses Between the Network Multiple Devices, Host Systems or Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses.

| UNIT-III | DEVICE DRIVERS AND INTERRUPTS SERVICING MECHANISM | Classes:10 |
|---|---|---|

Device Drivers, Parallel Port and Serial Port Device Drivers in a System, Device Drivers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

| UNIT-IV | PROGRAMMING CONCEPTS | Classes:10 |
|---|---|---|

**Instruction Sets:** Introduction, preliminaries, ARM processor, SHARC processor.

**Embedded Programming in C, C++, VC++ and JAVA:** Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

| UNIT-V | HARDWARE- SOFTWARE C0- DESIGN IN AN EMBEDDED SYSTEM | Classes:10 |
|---|---|---|

Embedded System Project Management, Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, use of Target Systems, use of Software Tools for Development of an Embedded System, use of Scopes and Logic Analysis for System, Hardware Tests. Issues in Embedded System Design.

**Text Books:**

1. Rajkamal, Embedded systems: Architecture, Programming and Design, TMH, 2008.

2. Wayne wolf, Computers as a component: principles of embedded computing system design.

**Reference Books:**

1. Arnold S Berger, Embedded System Design, 1st ed., CMP Books, 2001.
2. An embedded software primer by David Simon, 1st Indian Reprint, PEA, 2001.
3. Steve Heath, Embedded systems design: Real world design , Newton Mass USA, 2002.

**Web References:**

1. https://www.slideshare.net/yayavaram/introduction-to-embedded-systems-2614825
2. https://pdfs.semanticscholar.org/a24e/c6903e740a61af9310efda3b7af8cdd00401.pdf

**E-Text Books:**

1. Qing Li, Caroline Yao, Real-Time Concepts for Embedded Systems, CRC Press, 2003.
2. Barrett,Embedded Systems: Design and Applications, Pearson Education, 2008.

**Outcomes:**

1. Describe the differences between the general computing system and the embedded system, also recognize the classification of embedded systems..
2. Design real time embedded systems using the concepts of RTOS.
3. To understand the processor and memory organization in an embedded system.
4. To learn the basic instruction set of ARM, SHARC processor and programming concepts.
5. To study devices and buses used in embedded system.
6. To understand the concept of Hardware- Software C0- Design in an Embedded System

# VLSI TECHNOLOGY AND DESIGN
## (Elective – I)

| M.Tech I Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Course code | Category | Hours/week | | | Credits | Maximum Marks | | |
| 18ES103 | Core | L | T | P | C | CIA | SEE | TOTAL |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| Contact Classes:50 | Tutorial Classes: - | Practical Classes: Nil | | | Total Classes:50 | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To learn the basic MOS Circuits
II. To learn the MOS Process Technology
III. To understand the operation of MOS devices.
IV. To impart in-depth knowledge about analog and digital CMOS circuits

| UNIT-I | INTRODUCTION | Classes:10 |
|---|---|---|

**Review of Microelectronics and Introduction to MOS Technologies:** (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

**Basic Electrical Properties of MOS, CMOS & BICOMS Circuits**: Ids -Vds Relationships, Threshold Voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, Zpu/Zpd, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

| UNIT-II | LAYOUT DESIGN | Classes:10 |
|---|---|---|

**Layout Design and Tools:** Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

**Logic Gates & Layouts:** Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

| UNIT-III | COMBINATIONAL LOGIC NETWORKS | Classes:10 |
|---|---|---|

Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

| UNIT-IV | SEQUENTIAL SYSTEMS | Classes:10 |
|---|---|---|

Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

| UNIT-V | DESIGN AND PLANNING | Classes:10 |
|---|---|---|

**Floor Planning & Architecture Design:** Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

**Introduction to CAD Systems (Algorithms) and Chip Design:** Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies-A simple Design Example.

**Text Books:**


1. K. Eshraghianet . al( 3 authors), Essentials of VLSI Circuits and Systems, , PHI of India Ltd.,2005
2. Wayne Wolf, Modern VLSI Design, 3rd ed., Pearson Education,2005.

**Reference Books:**

1. N.H.E Weste, K.Eshraghian, Adison Wesley, Principals of CMOS Design, 2nd ed.,1993
2. Fabricius, Introduction to VLSI Design, MGH International Edition, 1990.
3. Baker, Li Boyce, CMOS Circuit Design, Layout and Simulation, PHI, 2004.

**Web References:**

1. http://www.csit-sun.pub.ro/courses/vlsi/Modern_VLSI_Design.pdf
2. https://electronicsforu.com/resources/learn-electronics/vlsi-developments-ic-fabrication

**E-Text Books:**

1. Wayne wolf, Prentice Hall, 2008
2. Pucknell and Eshraghian, Basic VLSI Design, 2004

**Outcomes:**

1. To be aware about the trends in semiconductor technology, and how it impacts scaling and performance
2. To understand MOS transistor as a switch and its capacitance
3. learn Layout, Stick diagrams, Fabrication steps, Static and Switching characteristics of inverters
4. Design, built and debug complex combinational and sequential circuits based on an abstract functional specification.
5. Synthesis of digital VLSI systems from register-transfer or higher level descriptions in hardware design languages.
6. Student will be able to design digital systems using MOS circuits.

# EMBEDDED COMPUTING
## (Elective – I)

| M.Tech I Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES104** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To make students familiar with the basic concepts and terminology of the target area, the embedded systems design flow.
II. To give students an understanding of the embedded system architecture.
III. To acquaint students with methods of executive device control and to give them opportunity to apply and test those methods in practice;
IV. To teach students to make measurements with the specified accuracy.

| UNIT-I | PROGRAMMING ON LINUX PLATFORM | Classes:10 |
|---|---|---|

System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. Operating System Overview: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue

| UNIT-II | INTRODUCTION TO SOFTWARE DEVELOPMENT TOOLS | Classes:10 |
|---|---|---|

GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

| UNIT-III | INTERFACING MODULES | Classes:10 |
|---|---|---|

Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

| UNIT-IV | NETWORKING BASICS | Classes:10 |
|---|---|---|

Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

| UNIT-V | IA32 INSTRUCTION SET | Classes:10 |
|---|---|---|

Application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

**Text Books:**


1. Peter Barry and Patrick Crowley, Modern Embedded Computing, 1st Ed., Elsevier/Morgan Kaufmann,2012.
2. Michael K. Johnson, Erik W. Troan, Linux Application Development, Adission Wesley, 1998.
3. Kip R. Irvine, Assembly Language for x86 Processors.


**Reference Books:**


1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens

**Web References:**

1.https://www.researchgate.net/publication/4240547_Embedded_Systems_Integration_Using_Web_Services

2. https://scss.tcd.ie/publications/tech-reports/reports.10/TCD-CS-2010-05.pdf

**E-Text Books:**

1. Carl Hamacher, ZvonkoVranesic, SafwatZaky, NaraigManjikianPucknell and Eshraghian, Computer Organization and Embedded Systems,Mc-Graw Hill Education, 2017

**Outcomes:**

1. Able to learn programming on LINUX platform.
2. Understand the Operating System Overview
3. Learn Software Development Tools
4. Analyze the interfacing modules and openCV for machine vision
5. Get knowledge on TCP/IP,UDP and other networking basics.
6. Understand IA32 instruction set

# ADVANCED OPERATING SYSTEMS
## (Elective – I)

| M.Tech I Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES105** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To learn the fundamentals of Operating Systems
II. To gain knowledge on Distributed operating system concepts that includes architecture,
III. Mutual exclusion algorithms, Deadlock detection algorithms and agreement protocols
IV. To gain insight on to the distributed resource management components viz. the algorithms for implementation of distributed shared memory, recovery and commit protocols
V. To know the components and management aspects of Real time, Mobile operating Systems.

| UNIT-I | INTRODUCTION TO OPERATING SYSTEMS | Classes:10 |
|---|---|---|

Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System.

| UNIT-II | INTRODUCTION TO UNIX AND LINUX | Classes:10 |
|---|---|---|

Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations.

| UNIT-III | SYSTEM CALLS | Classes:10 |
|---|---|---|

System calls and related file structures, Input / Output, Process creation & termination. Inter Process Communication Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

| UNIT-IV | INTRODUCTION TO DISTRIBUTED SYSTEMS | Classes:10 |
|---|---|---|

Goals of distributed system, Hardware and software concepts, Design issues. Communication in Distributed Systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

| UNIT-V | SYNCHRONIZATION IN DISTRIBUTED SYSTEMS | Classes:10 |
|---|---|---|

Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

**Text Books:**


1. Maurice J. Bach, The design of the UNIX Operating Systems, PHI, 1986.
2. Andrew. S. Tanenbaum, Distributed Operating System, PHI, 1994.
3. Richard Peterson, The Complete reference LINUX, 4th Ed., McGraw – Hill.
4. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.

**Reference Books:**

1. Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
2. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
3. UNIX User Guide – Ritchie & Yates.
4. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

**Web References:**

1. https://en.wikipedia.org/wiki/Operating_system

**E-Text Books:**

1. Silberschatz, Galvin, Gagne: Operating System Concepts, 8th Edition, Wiley, 2008
2. Andrew S. Tanenbaum, Albert S. Woodhull: Operating Systems, Design and Implementation, 3rd Edition, Prentice Hall, 2006.
3. Pradeep K Sinha: Distribute Operating Systems, Concept and Design, PHI, 2007

**Outcomes:**

1. Master functions, structures and history of operating systems
2. Understand the concepts of UNIX and LINUX
3. Learn process creation and termination
4. study the inter process communication and client server example
5. Learn the goals of distributed system and design issues
6. Understand the algorithms of synchronization in distributed systems

# DSP PROCESSORS AND ARCHITECTURES
## (Elective – II)

| M.Tech I Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES106** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To give an exposure to the various fixed point & a floating point DSP architectures

II. To develop applications using these processors.

| UNIT-I | INTRODUCTION | Classes:10 |
|---|---|---|

Introduction, Digital signal- processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT),Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

**Computational Accuracy in DSP Implementations:**

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

| UNIT-II | ARCHITECTURES AND EXECUTION | Classes:10 |
|---|---|---|

**Architectures for Programmable DSP Devices:**

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

**Execution Control and Pipelining:**

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

| UNIT-III | IMPLEMENTATION OF DSP | Classes:10 |
|---|---|---|

**Programmable Digital Signal Processors:**

Commercial Digital signal – processing Devices, Data Addressing modes of TMS320C54XXDSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control,TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

**Implementations of Basic DSP Algorithms:**

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

| UNIT-IV | IMPLEMENTATION OF FFT ALGORITHMS | Classes:10 |
|---|---|---|

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

| UNIT-V | INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES | Classes:10 |
|---|---|---|

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

**Text Books:**

1. Avtar Singh and S. Srinivasan, Digital Signal Processing, Thomson Publications, 2004.
2. Lapsleyetal, DSP Processor Fundamentals, Architectures & Features, S.Chand& Co, 2000.

**Reference Books:**

1. B. VenkataRamani, M. Bhaskar, Digital Signal Processors, Architecture, Programming and Applications, 4th ed. Reprint,TMH,2008.
2. Jonatha Stein, Digital Signal Processing ,1st ed., John Wiley, 2005

**Web References:**

1. https://en.wikipedia.org/wiki/Digital_signal_processor
2. https://ieeexplore.ieee.org/document/6771184

**E-Text Books:**

1. Kuo, Digital Signal Processors: Architectures, Implementations, and Applications, Pearson Education India, 2005
2. Phil Lapsley, Jeff Bier, AmitShoham, Edward A. Lee, DSP Processor Fundamentals: Architectures and Features, Wiley India Pvt Ltd, 2009.

**Outcomes:**

1. Comprehends the knowledge & concepts of digital signal processing techniques.
2. Learn the DSP programming tools and use them for applications
3. Students will be able to use the DSP processors TMS 320C 54XX for implementation of DSP algorithms & its interfacing techniques with various I/O peripherals.
4. Students will be able to use MATLAB DSP toolbox for analysis & design of DSP.
5. Acquire knowledge of DSP computational building blocks and knows how to Achieve speed in DSP architecture or processor.
6. Learn the architecture details and instruction sets of fixed and floating point DSPs

# CMOS DIGITAL INTEGRATED CIRCUIT DESIGN
## (Elective – II)

| M.Tech I Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES107** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To lay good foundation on the design and analysis of CMOS digital integrated circuits.

II. To study digital circuits using various logic methods and their limitations.

| UNIT-I | CMOS DESIGN | Classes:10 |
|---|---|---|

**CMOS inverters** -static and dynamic characteristics.

**Static and Dynamic CMOS design-** Domino and NORA logic - combinational and sequential circuits.

| UNIT-II | CIRCUITS AND SIZING OF TRANSISTOR | Classes:10 |
|---|---|---|

**Method of Logical Effort for Transistor Sizing** -power consumption in CMOS gates- Low power CMOS design.

**Arithmetic Circuits in CMOS VLSI** - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

| UNIT-III | BIPOLAR GATE DESIGN | Classes:10 |
|---|---|---|

BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.

| UNIT-IV | LAYOUT DESIGN RULES | Classes:10 |
|---|---|---|

Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

| UNIT-V | SUBSYSTEM DESIGN PROCESS | Classes:10 |
|---|---|---|

General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

**Text Books:**


1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, 2nded.,MGH,1999.
2. Jan M Rabaey, Digital Integrated Circuits-ADesign Perspective,2nded.Prentice Hall,2003.
3. Eugene D Fabricus, Introduction to VLSI Design, McGraw Hill International Edition, 1990.


**Reference Books:**


1. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000.
2. Neil H E West and Kamran Eshranghian, Principles of CMOS VLSI Design: A System Perspective",2nd ed., Addision-Wesley,2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation,IEEE Press, 1998.
4. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital

5. Integrated Circuits, 3rd ed., McGraw-Hill, 2004

**Web References:**

1. https://www.u-cursos.cl/usuario/9553d43f5ccbf1cca06cc02562b4005e/mi_blog/r/CMOS_Circuit_Design__Layout__and_Simulation__3rd_Edition.pdf
2. http://www.roletech.net/books/DigitalIntegratedCircuit.pdf

**E-Text Books:**

1. Sung-Mo (Steve) Kang, Yusuf Leblebici, McGraw-Hill Higher Education; 41 edition, 2002
2. Hubert Kaeslin, Cambridge University Press, 2008

**Outcomes:**

1. To study about CMOS inverters and its applications
2. To design low power CMOS circuits
3. To analyze the Bi-CMOS logic circuits
4. To study the layout design rules for designing the circuits
5. To study the static and dynamic characteristics of CMOS inverters
6. To analyze the ALU sub-system design

# EMBEDDED C
## (Elective – II)

<table>
<tr><td colspan="9">M.Tech I Semester: EMBEDDED SYSTEM</td></tr>
<tr><td colspan="2">Course code</td><td>Category</td><td colspan="3">Hours/week</td><td>Credits</td><td colspan="2">Maximum Marks</td></tr>
<tr><td colspan="2" rowspan="2">18ES108</td><td rowspan="2">Core</td><td>L</td><td>T</td><td>P</td><td>C</td><td>CIA</td><td>SEE</td><td>TOTAL</td></tr>
<tr><td>4</td><td>-</td><td>-</td><td>4</td><td>40</td><td>60</td><td>100</td></tr>
<tr><td colspan="2">Contact Classes:50</td><td colspan="2">Tutorial Classes: -</td><td colspan="3">Practical Classes: Nil</td><td colspan="2">Total Classes:50</td></tr>
<tr><td colspan="9">OBJECTIVES:<br>The course should enable the students to :<br>I. Presents practical lessons and techniques for use in Designing, Implementing, Integrating and Testing software for Modern Embedded Systems<br>II. Describes what an embedded system is, what makes them different, and what embedded systems designers need to know to develop embedded systems<br>III. Provides the student with a life cycle view for designing multi-objective, multi-discipline embedded systems<br>IV. Imparts a solid understanding of the role of embedded systems and embedded systems design and development in modern day's technology-enabled society</td></tr>
<tr><td colspan="2">UNIT-I</td><td colspan="5">PROGRAMMING EMBEDDED SYSTEMS IN C</td><td colspan="2">Classes:10</td></tr>
<tr><td colspan="9">Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions.</td></tr>
<tr><td colspan="2">UNIT-II</td><td colspan="5">INTRODUCING THE 8050 MICROCONTROLLER FAMILY</td><td colspan="2">Classes:10</td></tr>
<tr><td colspan="9">Introduction, What's in a name, The external interface of the Standard 8050, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption,Conclusions.</td></tr>
<tr><td colspan="2">UNIT-III</td><td colspan="5">READING SWITCHES</td><td colspan="2">Classes:10</td></tr>
<tr><td colspan="9">Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions.</td></tr>
<tr><td colspan="2">UNIT-IV</td><td colspan="5">ADDING STRUCTURE TO THE CODE</td><td colspan="2">Classes:10</td></tr>
<tr><td colspan="9">Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions.</td></tr>
<tr><td colspan="2">UNIT-V</td><td colspan="5">MEETING REAL-TIME CONSTRAINTS</td><td colspan="2">Classes:10</td></tr>
<tr><td colspan="9">Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions.</td></tr>
<tr><td colspan="9">Text Books:<br>1. Michael J. Pont, "Embedded C", 2nd Edition, Pearson Education, 2008</td></tr>
</table>

**Reference Books:**

1. Nigel Gardner, “PIC micro MCU C-An introduction to programming”, The Microchip PIC in CCS C

**Web References:**

1. http://web.eecs.umich.edu/~jfr/embeddedctrls/files/C_review_jac_ETH.pdf
2. http://stepsmail.com/download/Career-In-Embedded-System.PDF

**E-Text Books:**

1. Tony Givargis Frank VahidHubert Kaeslin,Embedded System Design: A Unified Hardware / Software Introduction, Wiley, 2006.
2. Furber,ARM System on Chip Architecture, Pearson, 2012

**Outcomes:**

1. Understand basic interfacing programming with 8050 microcontroller
2. Learn different ways of reading ports
3. Learn Object-oriented programming with C
4. Work on Real-Time Constraints

# RESEARCH METHODOLOGY AND IPR

| M.Tech I Semester: Common to all Branches | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18AS101** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | 0 | 0 | 4 | 40 | 60 | 100 |
| **Contact Classes:60** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:60** | | | |

**OBJECTIVES:**

**The course should enable the students to:**

1. Understand research problem formulation.
2. Analyze research related information
3. Follow research ethics
4. Understand that today's world is controlled by computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
5. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
6. Understand the IOR protection provides an incentive to inventors for further research work and investment in R&D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

| **UNIT-I** | **Classes:12** |
|---|---|

**Research Methodology:**

Meaning of research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowledge how Research is done, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India.

**Research Design:**

Meaning of Research Design, Need for Research Design, Features of Good Design, Important concepts relating to Research Design, Different Research Designs, Basic principles of experimental designs.

| **UNIT-II** | **Classes:12** |
|---|---|

**Methods of Data Collection:**

Collection of Primary Data, Observation Method, Interview Method, Collection of Data through Questionnaires, Collection of Data through Schedules, Difference between Questionnaires and Schedules, Some other methods of data collection, Collection of secondary data, Selection of appropriate method for data collection, Case study method.

| **UNIT-III** | **Classes:12** |
|---|---|

**Testing of Hypotheses:**

What is a Hypothesis, Basic concepts concerning testing of hypothesis, Procedure for hypothesis testing, Flow diagram for hypothesis testing, Measuring the power of a hypothesis test, Tests of hypotheses, Importance of Parametric Tests, Hypothesis testing of means, Hypothesis testing for differences between means, Hypothesis testing for comparing two related samples, Hypothesis testing of proportions, Hypothesis testing for difference between proportions, Hypothesis testing for comparing a variance some hypothesized population variance, Testing and equality of variances of two normal populations, Hypothesis testing of correlation coefficients, Limitations of the tests of Hypotheses.

| UNIT-IV | Classes:12 |
|---|---|
| **Interpretation and Report Writing:**<br>Meaning of Interpretation, Why Interpretation?, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different steps in writing report, Layout of the Research Project, Types of reports, Oral presentation, Mechanics of writing a research report, Precautions for writing research reports. | |
| **UNIT-V** | **Classes:12** |
| **Intellectual Property Rights:**<br>Module I- Introduction<br>1) Intellectual property: meaning, nature and significance<br>2) Various forms of intellectual properties: copyright, patent, trademark, design, geographical indication, semiconductor and plant variety<br>3) Major international instruments relating to the protection of intellectual properties<br>Module II- Copyright<br>1) Copyright: meaning ,scope<br>2) Subject matter of copyright: original literary, dramatic, musical, artistic works; cinematograph films and sound recordings<br>3) Ownership of copyright , Assignment and licence of copyright<br>4) Infringement and exceptions of infringement of copyright and remedies against infringment of copyright: civil, criminal and administrative.<br>Module III – Trade Marks<br>1. Trade mark: meaning,scope<br>2. Absolute and relative grounds of refusal<br>3. Doctrine of honest concurrent user<br>4. Procedure for registration and term of protection<br>5. Rights of holder and assignment and licensing of marks<br>6. Infringement and remedies<br>7. Trade marks registry and appellate board<br>Module IV- Patents<br>1. Patent: meaning<br>2. Criteria for patentability and non-patentable inventions<br>3. Procedure for registration and term of protection<br>4. Grants of patent, rights of patentee and revocation of patent<br>5. Compulsory licence and government use of patent<br>6. Infringement, exceptions to infringement of patent and remedies<br>7. Patent office and Appellate Board | |
| **Text Books**<br>1. Kothari. C.R, 1990,"Research methodology: Methods and Techniques. New Age International, 418P<br>2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"<br>3. Ranjit Kumar, 2nd Edition, "Research Methodology: A step by Step Guide for beginers" | |
| **Reference Books:**<br>1. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd. 2007<br>2. Mayall, "Industrial Design", McGraw Hill, 1974.<br>3. Niebel, "Product Design", McGraw Hill, 1974.<br>4. Asimov, "Introduction to Design", Prentice Hall, 1962. | |

5. Robert P.Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.
6. T.Ramappa, "Intellectual Property Rights Under WTO", S.Chand, 2008

## MICROCONTROLLERS AND INTERFACING LABORATORY

**M.Tech I Semester – EMBEDDED SYSTEM**

| Course Code | Category | Hours / Week | | | Credits | Maximum Marks | | |
|---|---|---|---|---|---|---|---|---|
| | | L | T | P | C | CIA | SEE | Total |
| 18ES110 | Core | - | - | 4 | 2 | 25 | 50 | 75 |
| Contact Classes: Nil | Tutorial Classes: Nil | Practical Classes: 39 | | | Total Classes: 39 | | | |

**OBJECTIVES:**

**The course should enable the students to:**

I. To have knowledge about the basic working of a microcontroller system and its programming in assembly language.

II. To provide experience to integrate hardware and software for microcontroller applications systems

**LIST OF EXPERIMENTS**

| | |
|---|---|
| **Expt. 1** | **WRITE A PROGRAM TO A) CLEAR THE REGISTER AND B) ADD 3 TO REGISTER TEN TIMES AND PLACE THE RESULT INTO MEMORY USE THE INDIRECT INSTRUCTIONS TO PERFORM LOOPING.** |
| It is a simple explanatory ALP using 8051 addressing modes. | |
| **Expt. 2** | **A DOOR SENSOR IS CONNECTED TO RB1 PIN AND A BUZZER IS CONNECTED TO RB7. WRITE A PROGRAM TO MONITOR DOOR SENSOR AND WHEN IT OPEN, SOUNDS THE BUZZER BY SENDING A SQUARE WAVE OF FEW HUNDRED HZ FREQUENCY TO IT.** |
| It is a simple embedded application focus on interfacing door sensor and a buzzer with micro controller | |
| **Expt. 3** | **WRITE A PROGRAM TO TOGGLE ALL THE BITS OF PORT B PARTS CONTINUOUSLY WITH A 250NS DELAY.** |
| This experiment focuses on control the port B bits using keil IDE | |
| **Expt. 4** | **STEPPER MOTOR CONTROL USING MICROCONTROLLER** |
| This experiment focuses to interface stepper motor which rotates as per the instructions loaded to microcontroller | |
| **Expt. 5** | **ELEVATOR INTERFACE** |
| This experiment focuses to interface elevator to the micro controller using keil IDE | |
| **Expt. 6** | **KEY BOARD INTERFACE** |
| This experiment focuses to interface keyboard to the micro controller using keil IDE | |

| | |
|---|---|
| **Expt. 7** | **LED INTERFACE** |
| This experiment focuses to interface LED to the micro controller to blink as per instruction using keil IDE | |
| **Expt. 8** | **TEMPERATURE SENSOR** |
| This experiment focus to interface Temperature sensor to the microcontroller to display the temperature | |
| **Expt. 9** | **SORT RTO'S ON TO 89C50 BOARD** |
| This experiment focus to install RTOS into 89C51 board | |
| **Expt. 10** | **SAMPLE THE SIGNAL USING ADC AND RECONSTRUCT BY USING DAC** |
| This Experiment focus on Signal Analog to digital conversion and vice versa | |

**Reference Books:**


1. Jonathan W. Valvano – Brookes / Cole, Embedded Microcomputer Systems, Real Time Interfacing,Thomas Learning, 1999.


**Web References:**

1. https://en.wikipedia.org/wiki/Embedded_system
2. https://www.springer.com/in/book/9781402083921

**Course Home Page:**

**SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 36 STUDENTS:**
**SOFTWARE:-**
**HARDWARE:** Intel 8086/8088, ARM, ST7 Lite Microcontrollers

**Course Outcome:**

At the end of the course, a student will be able to:

1. Familiarize with the assembly level programming using keil software
2. Design circuits for various applications using microcontrollers
3. An in-depth knowledge of applying the concepts on real- time applications

## VLSI DESIGN LABORATORY

| M.Tech I Semester – EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course Code** | **Category** | **Hours / Week** | | | **Credits** | **Maximum Marks** | | |
| | | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **Total** |
| 18ES111 | Core | - | - | 4 | 2 | 25 | 50 | 75 |
| **Contact Classes: Nil** | **Tutorial Classes: Nil** | **Practical Classes: 39** | | | | **Total Classes: 39** | | |

**OBJECTIVES:**

**The course should enable the students to:**

I. To lay good foundation on the design and analysis of CMOS digital integrated circuits.
II. To study digital circuits using various logic methods and their limitations.

**LIST OF EXPERIMENTS**

| | |
|---|---|
| **Expt. 1** | **DESIGN AND SIMULATION OF ARITHEMATIC /LOGIC OPERATOR CIRCUITS USING VERILOG/VHDL** |
| This experiment is focusing on basic arithmetic & logical operation implementation | |
| **Expt. 2** | **MODELING OF COMBINATIONAL/SEQUENTIAL CIRCUITS USING VERILOG HDL** |
| This experiment is focusing on modeling of Combinational & sequential circuits | |
| **Expt. 3** | **SIMULATION OF SCHEMATIC /RTL USING XILINX ISE TOOL** |
| To perform simulation using modern Xilinx tool for schematic verification | |
| **Expt. 4** | **ARBITER DESIGN USING STATE DIAGRAM IN XILINX ISE TOOL** |
| To design & simulate arbiter using state diagram | |
| **Expt. 5** | **SIMULATION OF HDL NETLIST USING TEST BENCH** |
| To simulate the netlist using test bench | |
| **Expt. 6** | **MODELING OF MAC UNIT USING VERILOG / VHDL** |
| To perform the model of MAC unit using Xilinx/VHDL | |
| **Expt. 7** | **MODELING OF ALU USING VERILOG / VHDL** |
| To perform the model of ALU unit using Xilinx/VHDL | |
| **Expt. 8** | **DESIGN AND 8-BIT SIGNED MULTIPLICATION ALGORITHM USING VERILOG / VHDL** |
| To perform multiplication of two 8-bit signed numbers | |

| Expt. 9 | DESIGN AND TECHNOLOGICAL MAPPING OF RTL NETLIST IN XILINX ISE TOOL |
|---|---|

To map the RTL Netlist in Xilinx ISE tool

**Reference Books:**


1. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000.
2. Neil H E West and Kamran Eshranghian, Principles of CMOS VLSI Design: A System Perspective",2nd ed., Addision-Wesley,2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation,IEEE Press, 1998.
4. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital
5. Integrated Circuits, 3rd ed., McGraw-Hill, 2004


**Web References:**

1. https://www.u-cursos.cl/usuario/9553d43f5ccbf1cca06cc02562b4005e/mi_blog/r/CMOS_Circuit_Design__Layout__and_Simulation__3rd_Edition.pdf
2. http://www.roletech.net/books/DigitalIntegratedCircuit.pdf

**Course Home Page:**

**SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 36 STUDENTS:**

**SOFTWARE:** Mentor Graphic tools / Cadance tools/ Synophysis tools. (180 nm Technology and Above)

**HARDWARE:** Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

**Course Outcome:**

At the end of the course, a student will be able to:

1. Apply theory and practice for designing digital logic circuits and logic system designs
2. Familiarize with the VHDL using Xilinx
3. Verify the design logic of combinational and sequential circuit
4. Simulate timing analysis and to calculate critical path time
5. Programming on FPGA for different digital logic circuits

# FPGA ARCHITECTURE AND APPLICATIONS

| M.Tech II Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES201** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. Familiarization of various complex programmable Logic devices of different families.
II. To study Field programmable gate arrays and realization techniques.
III. To study different case studies using one hot design methods.

| UNIT-I | INTRODUCTION | Classes:10 |
|---|---|---|

**Programmable Logic:** ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

**FPGA:** Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

| UNIT-II | FINITE STATE MACHINES (FSM) | Classes:10 |
|---|---|---|

**Case Studies:** Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

| UNIT-III | REALIZATION OF STATE MACHINE | Classes:10 |
|---|---|---|

Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

| UNIT-IV | FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN | Classes:10 |
|---|---|---|

Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

| UNIT-V | DIGITAL FRONT END DIGITAL DESIGN TOOLS FOR FPGAS & ASICS | Classes:10 |
|---|---|---|

Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

**Text Books:**


1. P.K.Chan& S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall, 1994.
2. S.Trimberger , Field Programmable Gate Array Technology, Kluwer Academic Publications,1994.

**Reference Books:**

1. John V. Oldfield, Richard C. Dorf, "Field Programmable Gate Arrays", Wiley India.

**Web References:**

1. https://www.edgefx.in/fpga-architecture-applications/
2. https://en.wikipedia.org/wiki/Field-programmable_gate_array

**E-Text Books:**

1. Christophe Bobda, Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications, Springer, 2010.

**Outcomes:**

1. Able to gain the knowledge about PLDs, FPGA Design & architectures.
2. Students should be able to understand different types of FSM's
3. Different FSM techniques like ASM and One-hot Design method
4. Understand the various frontend design tools and implementation process.
5. Analyze System level Design and their application for Combinational and Sequential Circuits.

# REAL TIME OPERATING SYSTEMS

| M.Tech II Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES202** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To learn the fundamentals of Operating Systems

II. To know the components and management aspects of Real time, Mobile operating Systems.

| UNIT-I | INTRODUCTION | Classes:10 |
|---|---|---|

**Introduction to UNIX:** Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

**Real Time Systems:** Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

| UNIT-II | APPROACHES TO REAL TIME SCHEDULING | Classes:10 |
|---|---|---|

Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

| UNIT-III | OPERATING SYSTEMS | Classes:10 |
|---|---|---|

Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

| UNIT-IV | CASE STUDIES | Classes:10 |
|---|---|---|

**Fault Tolerance Techniques:** Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

**Case Studies – VX Works:** Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

| UNIT-V | RT LINUX | Classes:10 |
|---|---|---|

Process Management, Scheduling, Interrupt Management, and Synchronization

**Text Books:**


1. Richard Stevens, Advanced Unix Programming, 2nd ed., Addison-Wesley, 2005.
2. Jane W.S. Liu, Real Time Systems, 1st ed., Pearson Education, 2000
3. C.M.Krishna, KANG G. Shin, Real Time Systems, McGraw.Hill, 1997


**Reference Books:**


1. Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
2. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley.

**Web References:**

1. https://en.wikipedia.org/wiki/Operating_system

**E-Text Books:**

1. Silberschatz, Galvin, Gagne: Operating System Concepts, 8th Edition, Wiley, 2008
2. Andrew S. Tanenbaum, Albert S. Woodhull: Operating Systems, Design and Implementation, 3rd Edition, Prentice Hall, 2006.
3. Pradeep K Sinha: Distribute Operating Systems, Concept and Design, PHI, 2007

**Outcomes:**

1. To distinguish a real-time system from other systems.
2. To identify the functions of operating system.
3. To evaluate the need for real-time operating system.
4. To implement the real-time operating system principles.
5. To analyze the case studies like VX works, RT Linux.
6. To understand the fault tolerance techniques in real time operating systems.

# SYSTEM ON CHIP ARCHITECTURE
## (Elective – III)

| M.Tech II Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES203** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. Design, optimize, and program a modern System-on-a-Chip.
II. Decompose the task into parallel components that cooperate to solve the problem.
III. Characterize and develop real-time solutions.
IV. Implement both hardware and software solutions, formulate hardware/software tradeoffs, and perform hardware/software co-design.
V. Understand the system on a chip from gates to application software, including on-chip memories and communication networks, I/O interfacing, RTL design of accelerators, processors, firmware and OS/infrastructure software.
VI. Understand and estimate key design metrics and requirements including area, latency, throughput, energy, power, predictability, and reliability.

| UNIT-I | INTRODUCTION TO THE SYSTEM APPROACH | Classes:10 |
|---|---|---|

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

| UNIT-II | PROCESSORS | Classes:10 |
|---|---|---|

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

| UNIT-III | MEMORY DESIGN FOR SOC | Classes:10 |
|---|---|---|

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

| UNIT-IV | INTERCONNECT CUSTOMIZATION AND CONFIGURATION | Classes:10 |
|---|---|---|

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism

| UNIT-V | APPLICATION STUDIES / CASE STUDIES | Classes:10 |
|---|---|---|

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

**Text Books:**

1. Michael J. Flynn and Wayne Luk, Computer System Design System-on-Chip, Wiely India Pvt. Ltd.
2. Steve Furber, ARM System on Chip Architecture,2nd Ed., 2000, Addison Wesley Professional.

**Reference Books:**

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

**Web References:**

1. https://en.wikipedia.org/wiki/System_on_a_chip
2. http://www.laccei.org/LACCEI2004-Miami/papers2/ET_024.doc

**E-Text Books:**

1. Prof Steve Furber, ARM System-on-Chip Architecture, Addison Wesley, 2000
2. Ahmed Jerraya and Wayne Wolf, Multiprocessor Systems-on-Chips, Elsevier, 2004

**Outcomes:**

1. Modeling and simulation of digital VLSI systems using hardware design language
2. To understand SOC architecture and instruction set.
3. Explain how design platforms can be used for an efficient design process
4. To understand soc interconnect architectures and understand bus structures.
5. Describe the design process for complex systems-on-chip
6. To analyze the soc system memory and cache memory.

# CRYPTOGRAPHY AND NETWORK SECURITY
## (Elective – III)

| M.Tech II Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES204** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To understand basics of Cryptography and Network Security.
II. To be able to secure a message over insecure channel by various means.
III. To learn about how to maintain the Confidentiality, Integrity and Availability of data.
IV. To understand various protocols for network security to protect against the threats in the networks

| UNIT-I | INTRODUCTION | Classes:10 |
|---|---|---|

**Symmetric Ciphers:** Overview – classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

**Public – Key Encryption and Hash Functions:** Introduction to Number Theory, Public-Key Cryptography and RSA, Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

| UNIT-II | NETWORK SECURITY PRACTICE | Classes:10 |
|---|---|---|

Authentication Applications, Kerbors, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

**System Security:** Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

| UNIT-III | WIRELESS SECURITY | Classes:10 |
|---|---|---|

Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

**Secure Networking Threats:** Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

| UNIT-IV | ENCRYPTION TECHNIQUES | Classes:10 |
|---|---|---|

Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

| UNIT-V | DESIGNING SECURE NETWORKS | Classes:10 |
|---|---|---|

Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, the Difficulties of Secure Networking, Security Technologies, Emerging Security Technologies General Design Considerations, Layer 2 Security Considerations, IP Addressing Design

Considerations - ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

**Text Books:**

1. William Stallings, Cryptography and Network Security Principles And Practices, 3rd ed., PearsEducation, 2003.
2. Sean Convery, Network Security Architectures, 1st ed., Cisco Press, 2004.

**Reference Books:**

1. AtulKahate, Cryptography and Network Security,2nd ed., Tata McGraw Hill, 2003.
2. Bruce Schneier, Applied Cryptography, 2nd ed., John Wiley and Sons Inc, 1996.

**Web References:**

1. http://www.vssut.ac.in/lecture_notes/lecture1428550736.pdf
2. http://pubs.sciepub.com/iteces/3/1/1/index.html

**E-Text Books:**

1. King, T. and Newson, D, Data Network Engineering, Kluwer, 1999
2. Peterson, L. L. and Davie, B. S, Computer Networks: A Systems Approach, Morgan Kaufmann, 1996

**Outcomes:**

1. To identify common network security vulnerabilities/attacks
2. To explain the foundations of Cryptography and network security
3. To demonstrate detailed knowledge of the role of encryption to protect data.
4. To analyze security issues arising from the use of certain types of technologies.
5. To identify the appropriate procedures required to secure networks.
6. To analyze and design network security protocols.

# EMBEDDED NETWORKS
## (Elective – III)

| M.Tech II Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES205** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. Understand the main principles of real-time Communication
II. Use suitable principles and standards in design and evaluation of sensor networks and wireless communication protocols for small digital transmitters.
III. Design and implement software and system solutions for wireless embedded systems.

| UNIT-I | EMBEDDED COMMUNICATION PROTOCOLS | Classes:10 |
|---|---|---|

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

| UNIT-II | USB and CAN Bus | Classes:10 |
|---|---|---|

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors – Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

| UNIT-III | ETHERNET BASICS | Classes:10 |
|---|---|---|

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

| UNIT-IV | EMBEDDED ETHERNET | Classes:10 |
|---|---|---|

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

| UNIT-V | WIRELESS EMBEDDED NETWORKING | Classes:10 |
|---|---|---|

Wireless sensor networks – Introduction – Applications – Network Topology – Localization – Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

**Text Books:**


1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.


**Reference Books:**


1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series

– Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - BhaskarKrishnamachari¬, Cambridge press 2005.

**Web References:**

1.https://www.freertos.org/FreeRTOS-Plus/FreeRTOS_Plus_TCP/networking_basics.html

2. https://ieeexplore.ieee.org/document/7096291

**E-Text Books:**

1. Olaf Pfeiffer, Andrew Ayre, Christian Keydel, T,Embedded Networking with Can and Canopen, Copperhill Media Corporation, 2008

**Outcomes:**

1. Learn different type of communication protocols
2. Study the concepts of USB,CAN bus and a simple application
3. Learn the elements ,architecture and working principle of Ethernet
4. Study about the embedded Ethernet
5. Understand the concepts of Wireless Embedded Networking

# HARDWARE SOFTWARE CO-DESIGN
## (Elective – IV)

| M.Tech II Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES206** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. Analyze and explain the control-flow and data-flow of a software program and a cycle-based hardware description,

II. Transform simple software programs into cycle-based hardware descriptions with equivalent behavior and vice versa,

III. Partition simple software programs into hardware and software components, and create appropriate hardware-software interfaces to reflect this partitioning,

IV. Identify performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software components, and

V. Use simulation software to co-simulate software programs with cycle-based hardware descriptions.

| UNIT-I | CO-DESIGN AND SYNTHESIS | Classes:10 |
|---|---|---|

**Co-Design Issues:** Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

**Co-Synthesis Algorithms:** Hardware software synthesis algorithms: hardware- software partitioning distributed system co-synthesis.

| UNIT-II | PROTOTYPING AND EMULATION | Classes:10 |
|---|---|---|

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

| UNIT-III | TARGET ARCHITECTURES | Classes:10 |
|---|---|---|

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8050-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

| UNIT-IV | COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR | Classes:10 |
|---|---|---|

**Architectures:** Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

**Design Specification and Verification:** Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

| UNIT-V | LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN | Classes:10 |
|---|---|---|

System – level specification, design representation for system level synthesis, system level specification languages, Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

**Text Books:**

1. Jorgen Staunstrup, Wayne Wolf, Hardware / software co- design Principles and Practice, springer,2009.
2. Hardware / software co- design Principles and Practice, Kluwer Academic Publishers , 2002.

**Reference Books:**

1. Wayne Wolf, Readings in hardware/software co-design, Kluwer Academic Publishers., 2001.

**Web References:**

1.https://books.google.co.in/books/about/Hardware_Software_Co_Design_for_Data_Flo.html?id=ZHdId5u0GCYC&redir_esc=y

2. https://ieeexplore.ieee.org/document/6172642

**E-Text Books:**

1. DeMicheli, Giovanni, Sami, Mariagiovanna, Hardware/Software Co-Design, Springer, 2006
2. Patrick R. Schaumont, A Practical Introduction to Hardware/Software Codesign, 3rd Edition, Springer, 2010.

**Outcomes:**

1. Analyze hardware-software co-design problems for systems with moderate complexity.
2. Apply hardware-software co-design methods and techniques to practical problems.
3. Designing hardware-software co-design solutions through SoPC and similar technologies.
4. Applying different levels of abstractions and provide models for verification of the architecture and functionality for embedded co-design solutions.
5. Evaluate and compare quality solutions compared to for example: performance, cost, security, power consumption and size.
6. Partition and design space exploration with LYCOS

# TCP / IP INTERNETWORKING
## (Elective – IV)

| M.Tech II Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES207** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. Analyze and differentiate networking protocols used in TCP/IP protocol suite,
II. Implement the concepts of naming and addressing to Internet IPv4 and their extension to IPv6
III. Compare three routing protocols used in the Internet and implement two of them
IV. Interpret and exemplify multicast routing
V. Categorize problems such as reliable transport, data delay, congestion and flow control and describe at least three congestion control schemes used in TCP
VI. Interpret the Internet best-effort type of service and its improvements

| UNIT-I | NETWORK MODELS AND CONNECTING DEVICES | Classes:10 |
|---|---|---|

Layered Tasks, The OSI Model, Layers in OSI Model, TCP/IP Protocol suite, Addressing, Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, Backbone Networks.

| UNIT-II | INTERNETWORKING CONCEPTS | Classes:10 |
|---|---|---|

Principles of Internetworking, Connectionless Interconnection, Application Level Interconnection, Network Level Interconnection, Properties of the Internet, Internet Architecture, Interconnection through IP Routers TCP, UDP & IP: TCP Services, TCP Features, Segment, A TCP Connection, Flow Control, Error Control, Congestion Control, Process to Process Communication, User Datagram, Checksum, UDP Operation, IP Datagram, Fragmentation, Options, IP Addressing: Classful Addressing

| UNIT-III | CONGESTION AND QUALITY OF SERVICE | Classes:10 |
|---|---|---|

Data Traffic, Congestion, Congestion Control, CongestionControl in TCP, Congestion Control in Frame Relay, Source Based Congestion Avoidance, DEC Bit Scheme, Quality of Service, Techniques to Improve QOS: Scheduling, Traffic Shaping, Admission Control, Resource Reservation, Integrated Services and Differentiated Services.

**Queue Management**: Concepts of Buffer Management, Drop Tail, Drop Front, Random Drop,Passive Buffer Management Schemes, Drawbacks of PQM, Active Queue Management: EarlyRandom Drop, RED Algorithm.

| UNIT-IV | STREAM CONTROL TRANSMISSION PROTOCOL | Classes:10 |
|---|---|---|

SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control. Mobile Network Layer: Entities and Terminology, IP Packet Delivery, Agents, Addressing, Agent Discovery, Registration, Tunneling and Encapsulating, Inefficiency in Mobile IP.

| UNIT-V | MOBILE TRANSPORT LAYER | Classes:10 |
|---|---|---|

Classical TCP Improvements, Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/Fast

Recovery, Transmission, Timeout Freezing, Selective Retransmission, Transaction Oriented TCP.

**Text Books:**

1. Behrouz A Forouzan, "TCP/IP Protocol Suite", 3rd Edition, TMH.
2. B.A. Forouzan, "Data communication & Networking", 4th Edition, TMH

**Reference Books:**

1. MahbubHasan& Raj Jain, " High performance TCP/IP Networking", PHI -2005
2. Douglas. E.Comer, "Internetworking with TCP/IP ", Volume I PHI
3. Larry L. Perterson and Bruce S. Davie , "Computer Networks- A Systems Approach", 2011, Morgan Kaufmann
4. JochenSchiiler, "Mobile Communications" , Pearson , 2nd Edition.

**Web References:**

1.https://www.oreilly.com/library/view/tcpip-guide/9781593270476/
2. http://ecomputernotes.com/computernetworkingnotes/multiple-access/tcpip-reference-model

**E-Text Books:**

1. Comer, Internetworking with TCP/IP, Pearson, 2015

**Outcomes:**

1. Know different layers of networks
2. Know internetworking concepts
3. Know the ways to control congestion using different algorithms
4. Learn stream control protocols
5. Learn mobile transport layer

# SOFTWARE DEFINES RADIO
## (Elective – IV)

| M.Tech II Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES208** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. The objective of this course is to provide knowledge of fundamental and state-ofthe art concepts in software defined radio.

| UNIT-I | INTRODUCTION TO SOFTWARE RADIO CONCEPTS | Classes:10 |
|---|---|---|

The need for Software radios and its definition, Characteristics and benefits of Software radio, Design principles of a software radio. Radio Frequency Implementation Issues: Purpose of RF front – end, Dynamic range, RF receiver front – end topologies, Enhanced flexibility of the RF chain with software radios, Importance of the components to overall performance, Transmitter architectures and their issues, Noise and distortion in the RF chain, ADC & DAC distortion, Pre-distortion, Flexible RF systems using micro-electromechanical systems.

| UNIT-II | MULTIRATE SIGNAL PROCESSING IN SDR | Classes:10 |
|---|---|---|

Sample rate conversion principles, Polyphase filters, Digital filter banks, Timing recovery in digital receivers using multirate digital filters.

| UNIT-III | DIGITAL GENERATION OF SIGNALS | Classes:10 |
|---|---|---|

Introduction, Comparison of direct digital synthesis with analog signal synthesis, Approaches to direct digital synthesis, Analysis of spurious signals, Spurious components due to periodic jitter, Bandpass signal generation, Performance of direct digital synthesis systems, Hybrid DDS – PLL Systems, Applications of direct digital synthesis, Generation of random sequences, ROM compression techniques.

| UNIT-IV | SMART ANTENNAS | Classes:10 |
|---|---|---|

Introduction, Vector channel modelling, Benefits of smart antennas, Structures for beamforming systems, Smart antenna algorithms, Diversity and Space time adaptive signal processing, Algorithms for transmit STAP, Hardware implementation of smart antennas, Array calibration, Digital Hardware Choices-Key hardware elements, DSP processors, FPGAs, Power management issues.

| UNIT-V | OBJECT ORIENTED REPRESENTATION OF RADIOS AND NETWORK | Classes:10 |
|---|---|---|

Networks, Object –oriented programming, Object brokers, Mobile application environments, Joint Tactical radio system. Case Studies in Software Radio Design: SPEAKeasy, JTRS, Wireless Information transfer system, SDR-3000 digital transceiver subsystem, Spectrum Ware, Brief introduction to Cognitive Networking.

**Text Books:**

1. Jeffrey Hugh Reed, "Software Radio: A Modern Approach to Radio Engineering," Prentice Hall Professional, 2002.

2. Paul Burns, “Software Defined Radio for 3G,” Artech House, 2002.

**Reference Books:**

1. Tony J Rouphael, “RF and DSP for SDR,” Elsevier Newnes Press, 2008.
2. P. Kenington, “RF and Baseband Techniques for Software Defined Radio,” Artech House, 2005.

**Web References:**

1. http://www.mprg.org/publications/pubs.shtml#Books
2. http://www.softradios.com/

**E-Text Books:**

1. Jeffery H.Reed, “Software Radio, (A modern approach to radio engineering)”, PHI PTR, 2002.
2. 2. John J. Rouphael, RF and Digital Signal Processing for Software Defined Radio, Elesiver, Newness Publications

**Outcomes:**

1. Understand the concepts of Software radio
2. Learn the Object oriented software radio and its configartion
3. Study of the digital generation of signals
4. Analyze the transmitter and receiver architectures
5. Identify the switches ,power amplifiers, technology and modeling
6. Analyze case studies in software radio design.

# RTOS AND FPGA LABORATORY

| M.Tech II Semester – EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course Code** | **Category** | **Hours / Week** | | | **Credits** | **Maximum Marks** | | |
| | | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **Total** |
| 18ES209 | Core | - | - | 4 | 2 | 25 | 50 | 75 |
| **Contact Classes: Nil** | **Tutorial Classes: Nil** | **Practical Classes: 39** | | | | **Total Classes: 39** | | |

**OBJECTIVES:**

**The course should enable the students to:**

I. Familiarize the RTOS System solution & tools
II. Study the Testing RTOS Environment and System Programming in keil and Tornado tools.
III. Implementation of Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)
IV. Implementation of Synthesis of Sequential Circuits

**LIST OF EXPERIMENTS**

| | |
|---|---|
| **Expt. 1** | **RTOS SYSTEM SOLUTION & TOOLS** |
| To get introduced to RTOS through Keil. | |
| **Expt. 2** | **TESTING RTOS ENVIRONMENT AND SYSTEM PROGRAMMING.**<br>**A) KEIL TOOLS**<br>**B) RTOS SYSTEM SOLUTIONS WITH TORNADO TOOLS.** |
| To get familiar with RTOS environment through Keil & Tornado tools. | |
| **Expt. 3** | **EMBEDDED DSP BASED SYSTEM DESIGNING.**<br>**A) CODE COMPRESSOR STUDIO (CCS) FOR EMBEDDED DSP USING TEXAS TOOL KIT.**<br>**B) ANALOG DSP TOOL KIT.** |
| To Design DSP System using CCS & Analog DSP tool kit | |
| **Expt. 4** | **SYNTHESIS OF THE DESIGNS MADE USING "VHDL / VERILOG AND MIXED DESIGN (VHDL & VERILOG)" AFTER SIMULATION IS TO BE VERIFIED USING FPGA/CPLD BLOCKS FROM DIFFERENT COMMERCIALLY AVAILABLE PRODUCTS ON:**<br>**A) SYNTHESIS OF 4 TO 6-MSI DIGITAL BLOCKS (COMBINATIONAL CIRCUITS)**<br>**B) SYNTHESIS OF SEQUENTIAL CIRCUITS – 6 TO 8 MSI AND 1 OR 2 VLSI CIRCUITS.** |
| To get familiar with synthesis process to combinational & Sequential Circuits | |

**Reference Books:**

1. Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
2. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley.

**Web References:**

1. https://en.wikipedia.org/wiki/Operating_system

**Course Home Page:**

**SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 36 STUDENTS:**

**SOFTWARE:** Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

**HARDWARE:** Mentor Graphic tools / Cadance tools/ Synophysis tools. (180 nm Technology and Above)

**Course Outcome:**

At the end of the course, a student will be able to:

1. Familiarize with the assembly level programming using keil software
2. Design circuits for various applications using microcontrollers
3. An in-depth knowledge of applying the concepts on real- time applications

## ADVANCED EMBEDDED SYSTEMS LABORATORY

| M.Tech II Semester – EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course Code** | **Category** | **Hours / Week** | | | **Credits** | **Maximum Marks** | | |
| | | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **Total** |
| 18ES210 | Core | - | - | 4 | 2 | 25 | 50 | 75 |
| **Contact Classes: Nil** | **Tutorial Classes: Nil** | **Practical Classes: 39** | | | | **Total Classes: 39** | | |

**OBJECTIVES:**

**The course should enable the students to:**

I. To enable the students to program, simulate and test the 8085, 8050, PIC 18 and ARM processor based circuits and their interfaces

II. To enable the students to program various devices using FLOWCODE, KIEL , MPLAB, XILINX ISE software

III. To provide a platform for the students to do multidisciplinary projects

**LIST OF EXPERIMENTS**

| | |
|---|---|
| **Expt. 1** | **PIC PROGRAMMING AND INTERFACING. PROGRAM FOR ADDITION OF BCD NUMBERS.** |
| To perform basic arithmetic programming | |
| **Expt. 2** | **INTERFACE AN LED ARRAY AND 7-SEGMENT DISPLAY** |
| To get familiar with interfacing of LED & 7 Segment display | |
| **Expt. 3** | **INTERFACING OF PIC WITH LCD** |
| To get familiar with interfacing of LCD. | |
| **Expt. 4** | **INTERFACING OF PIC WITH KEYBOARD INTERFACING** |
| To get familiar with interfacing of Keyboard. | |
| **Expt. 5** | **INTERFACING OF PIC WITH ADC, DAC** |
| To get familiar with interfacing of ADC & DAC | |
| **Expt. 6** | **INTERFACING OF PIC WITH TEMPERATURE SENSOR** |
| To get familiar with interfacing of Temperature sensor. | |
| **Expt. 7** | **INTERFACING OF PIC WITH RTC** |
| To get familiar with interfacing of Real Time Clock | |
| **Expt. 8** | **INTERFACING OF PIC WITH DC MOTOR CONTROL** |
| To get familiar with interfacing of DC motor | |

| | |
|---|---|
| **Expt. 9** | **INTERFACING OF PIC WITH STEPPER MOTORS** |
| To get familiar with interfacing of stepper motor | |
| **Expt. 10** | **ARM PROGRAMMING AND INTERFACING. INTRODUCTION TO ARM DEVELOPMENT TOOLS.** |
| To get familiar with interfacing of ARM Development tools. | |
| **Expt. 11** | **SIMPLE ARM ASSEMBLY LANGUAGE AND C PROGRAMMING USING ARM KITS.** |
| To get introduced with ARM Assembly Language & C- programming | |
| **Expt. 12** | **LCD INTERFACING.** |
| To get familiar with interfacing of LCD with ARM Processor. | |
| **Expt. 13** | **TIMER AND COUNTER PROGRAMMING.** |
| To get familiar with counter & timer programming | |
| **Expt. 14** | **INTERFACING WITH DATA CONVERTERS.** |
| To get familiar with interfacing of Data converters. | |
| **Expt. 15** | **SERIAL PORT PROGRAMMING.** |
| To get familiar with Serial Port programming. | |
| **Expt. 16** | **INTERFACING WITH SENSORS & MOTORS.** |
| To get familiar with interfacing with Sensor & Motor. | |
| **Expt. 17** | **GENERATION OF PWM.** |
| To get familiar with generation of PWM. | |

**Reference Books:**


1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series – Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - BhaskarKrishnamachari¬, Cambridge press 2005.


**Web References:**

1. https://www.freertos.org/FreeRTOS-Plus/FreeRTOS_Plus_TCP/networking_basics.html
2. https://ieeexplore.ieee.org/document/7096291

| |
|---|
| **Course Home Page:** |
| **SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 36 STUDENTS:**<br>**SOFTWARE:** Keil Software<br>**HARDWARE:** PIC, 8050 MC |
| **Course Outcome:**<br>At the end of the course, a student will be able to:<br>1. Familiarize with the ALP and C program using RTOS 8050 kits.<br>2. Dump the programs into the microcontroller kits using flash magic software.<br>3. Study ARM evaluation board and familiarize with basic programming concepts.<br>4. write programs to interface various I/O devices with PIC micro controllers |

## TERM PAPER

| M.Tech II Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES211** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 0 | 0 | 4 | 2 | 50 | - | 50 |
| **Contact Classes: Nil** | **Tutorial Classes: Nil** | | **Practical Classes:20** | | | **Total Classes:20** | | |

The Term Paper is a self study report and shall be carried out either during II semester along with other lab courses. Every student will take up this term paper individually and submit a report. The scope of the term paper could be an exhaustive literature review choosing any engineering concept with reference to standard research papers or an extension of the concept of earlier course work in consultation with the term paper supervisor. The term paper reports submitted by the individual students during the II semester shall be evaluated for a total of 50 marks for continuous assessment; it shall be conducted by two Examiners, one of them being term paper supervisor as internal examiner and an external examiner nominated by the Principal from the panel of experts recommended by HOD.

# EMBEDDED LINUX
## (Open Elective)

| M.Tech III Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES301** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To make the student work in Linux Desktop, gain knowledge on using software development, GNU tools in Linux, porting Linux kernel into hardware board, typically based on ARM processor.

II. Write application software and run it in the target board.

| UNIT-I | LINUX FUNDAMENTALS | Classes:10 |
|---|---|---|

Introduction - host-target development setup - hardware support - development languages and tools – RT Linux.

| UNIT-II | INITIALIZTION | Classes:10 |
|---|---|---|

Linux kernel and kernel initialization - system initialization – hardware support - boot loaders.

| UNIT-III | DEVICE HANDLING | Classes:10 |
|---|---|---|

Device driver basics - module utilities - file systems - MTD subsystems – busybox.

| UNIT-IV | DEVELOPMENT TOOLS | Classes:10 |
|---|---|---|

Embedded development environment - GNU debugger - tracing & profiling tools - binary utilities - kernel debugging - debugging embedded Linux applications - porting Linux - Linux and real time - SDRAM interface.

| UNIT-V | DEVICE APPLICATIONS | Classes:10 |
|---|---|---|

Asynchronous serial communication interface - parallel port interfacing - USB interfacing – memory I/O interfacing - using interrupts for timing.

**Text Books:**

1. KarimYaghmour, Jon Masters, Gillad Ben Yossef, Philippe Gerum, Building embedded Linux systems, O'Reilly, 2008.
2. Christopher Hallinan, Embedded Linux Primer: A practical real world approach, Prentice Hall, 2007.

**Reference Books:**

1. Craig Hollabaugh, "Embedded Linux: Hardware, software and Interfacing", Pearson Education, 2002.
2. Doug Abbott, "Linux for embedded and real time applications", Elsevier Science, 2003

**Web References:**

1. https://en.wikipedia.org/wiki/Linux
2. http://www.ijsrp.org/research-paper-1115/ijsrp-p4789.pdf

**E-Text Books:**

1. Hollabaugh, Embedded Linux, Pearson, 2002.

**Outcomes:**

1. To use Linux desktop and GNU tool chain with Eclipse IDE.
2. Cross compile Linux kernel and port it to target board.
3. Add applications and write customized application for the Linux kernel in the target board.

# FUNDAMENTALS AND APPLICATIONS OF MEMS
## (Open Elective)

| M.Tech III Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES302** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To study the essential material properties
II. To study various sensing and transduction technique
III. To know about the polymer and optical MEMS

| UNIT-I | INTRODUCTION TO MEMS | Classes:10 |
|---|---|---|

History of MEMS Development, Characteristics of MEMS-miniaturization - micro electronics integration -Mass fabrication with precision. Micro fabrication - microelectronics fabrication process- silicon based MEMS processes- new material and fabrication processing- points of consideration for processing.

| UNIT-II | PROPERTIES OF MEMS | Classes:10 |
|---|---|---|

Conductivity of semiconductors, crystal plane and orientation, stress and stain – definition – relationship between tensile stress and stain- mechanical properties of silicon and thin films, Flexural beam bending analysis under single loading condition- Types of beam- deflection of beam-longitudinal stain under pure bendingspring constant, torsional deflection, intrinsic stress, resonance and quality factor.

| UNIT-III | SENSING AND ACTUATION | Classes:10 |
|---|---|---|

Electrostatic sensing and actuation-parallel plate capacitor – Application-Inertial, pressure and tactile sensorparallel plate actuator- comb drive.

Thermal sensing and Actuations-thermal sensors-Actuators- Applications- Inertial, Flow and Infrared sensors.

Piezoresistive sensors- piezoresistive sensor material- stress in flexural cantilever and membraneApplication-Inertial, pressure, flow and tactile sensor. Piezoelectric sensing and actuation- piezoelectric material properties-quartz-PZT-PVDF –ZnOApplication-Inertial, Acoustic, tactile, flow-surface elastic waves

Magnetic actuation- Micro magnetic actuation principle- deposition of magnetic materials- Design and
fabrication of magnetic coil.

| UNIT-IV | BULK AND SURFACE MICROMACHINING | Classes:10 |
|---|---|---|

Anisotropic wet etching, Dry etching of silicon, Deep reactive ion etching (DRIE), Isotropic wet etching, Basic surface micromachining process- structural and sacrificial material, stiction and antistiction methods, Foundry process.

| UNIT-V | POLYMER AND OPTICAL MEMS | Classes:10 |
|---|---|---|

Polymers in MEMS- polymide-SU-8 liquid crystal polymer(LCP)-PDMS-PMMA-Parylene-Flurocorbon, Application-Acceleration, pressure, flow and tactile sensors. Optical MEMS-passive MEMS optical components-lenses-mirrors-Actuation for active optical MEMS.

**Text Books:**

1. Chang Liu, “Foundations of MEMS”, Pearson International Edition, 2006.

**Reference Books:**

1. GaberielM.Rebiz, RF MEMS Theory,Design and Technology, John Wiley & Sons,2003
2. Charles P.Poole, Frank J.Owens, Introduction to nanotechnology, John Wiley & sons, 2003.
3. Julian W.Gardner, Vijay K Varadhan, Microsensors, MEMS and Smart devices, John Wiley and sons, 2001.

**Web References:**

1. https://www.lboro.ac.uk/microsites/mechman/research/ipm-ktn/pdf/Technology_review/an-introduction-to-mems.pdf
2. https://www.slideshare.net/navinec1/micro-electromechanical-system-mems

**E-Text Books:**

1. VikasChoudhary and Krzysztof Iniewski, MEMS: Fundamental Technology and Applications ARM System-on-Chip Architecture, CRC Press, 2017

**Outcomes:**

1. The student will have a broad knowledge in MEMS devices
2. The student will have a broad knowledge in Microfluidic structures
3. Student will be able to understand different fabrication and packaging techniques

## AVAILABLE MOOCs
## (Open Elective)

<table>
<tr><td colspan="9">M.Tech III Semester: EMBEDDED SYSTEM</td></tr>
<tr><td>Course code</td><td>Category</td><td colspan="3">Hours/week</td><td>Credits</td><td colspan="3">Maximum Marks</td></tr>
<tr><td rowspan="2">18ES303</td><td rowspan="2">Core</td><td>L</td><td>T</td><td>P</td><td>C</td><td>CIA</td><td>SEE</td><td>TOTAL</td></tr>
<tr><td>4</td><td>0</td><td>0</td><td>4</td><td>40</td><td>60</td><td>100</td></tr>
<tr><td colspan="2">Contact Classes:-</td><td colspan="2">Tutorial Classes: -</td><td colspan="2">Practical Classes: Nil</td><td colspan="3">Total Classes:-</td></tr>
<tr><td colspan="9">Meeting with the global requirements, to inculcate the habit of self learning and incompliance with UGC guidelines, MOOC (Massive Open Online Course) courses have been introduced as electives. The main intension to introduce MOOCs is to obtain enough exposure through online tutorials, self-learning at one's own pace, attempt quizzes, discuss with professors from various universities and finally to obtain certificate of completion for the course from the MOOCs providers<br>Regulations for MOOCs<br>➢ The respective departments shall give a list from NPTEL or any other standard providers, whose credentials are endorsed by the HOD.<br>➢ Each department shall appoint Coordinators/Mentors and allot the students to them who shall be responsible to guide students in selecting online courses and provide guidance for the registration, progress and completion of the same.<br>➢ A student shall choose an online course (relevant to his/her programme of study) from the given list of MOOCs providers, as endorsed by the teacher concerned, with the approval of the HOD.<br>➢ The details of MOOC(s) shall be displayed in Grade card of a student, provided he/she submits the proof of completion of it to the department concerned through the Coordinator/Mentor.<br>➢ Student can get certificate from SWAYAM/NPTEL or any other standard providers, whose credentials are endorsed by the HOD. The course work should not be less than 12 weeks or student may appear for end examination conducted by the Institute.<br>➢ There shall be one Mid Continuous Internal Examination (Quiz exam for 40 marks) after 9 weeks of the commencement of the course and semester end examination (Descriptive exam for 60 marks) shall be done along with the other regular courses.<br>➢ Three credits will be awarded upon successful completion of each MOOC courses having minimum of 8 weeks duration.</td></tr>
</table>

# ADVANCED COMPUTER ARCHITECTURE
## (Elective – V)

| M.Tech III Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES304** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. Understand the micro-architectural design of processors

II. Learn about the various techniques used to obtain performance improvement and power savings in current processors

| UNIT-I | FUNDAMENTALS OF COMPUTER DESIGN | Classes:10 |
|---|---|---|

Review of Fundamentals of CPU, Memory and IO – Trends in technology, power, energy and cost, Dependability – Performance Evaluation

| UNIT-II | INSTRUCTION LEVEL PARALLELISM | Classes:10 |
|---|---|---|

ILP concepts – Pipelining overview – Compiler Techniques for Exposing ILP – Dynamic Branch Prediction – Dynamic Scheduling – Multiple instruction Issue – Hardware Based Speculation – Static scheduling – Multi-threading – Limitations of ILP – Case Studies.

| UNIT-III | DATA-LEVEL PARALLELISM | Classes:10 |
|---|---|---|

Vector architecture – SIMD extensions – Graphics Processing units – Loop level parallelism.

| UNIT-IV | THREAD LEVEL PARALLELISM | Classes:10 |
|---|---|---|

Symmetric and Distributed Shared Memory Architectures – Performance Issues – Synchronization – Models of Memory Consistency – Case studies: Intel i7 Processor, SMT & CMP Processors

| UNIT-V | MEMORY AND I/O | Classes:10 |
|---|---|---|

Cache Performance – Reducing Cache Miss Penalty and Miss Rate – Reducing Hit Time – Main Memory and Performance – Memory Technology. Types of Storage Devices – Buses – RAID – Reliability, Availability and Dependability – I/O Performance Measures.

**Text Books:**

1. John L Hennessey and David A Patterson, “Computer Architecture A Quantitative Approach”, Morgan Kaufmann/ Elsevier, Fifth Edition, 2012.

**Reference Books:**

1. Kai Hwang and Faye Briggs, “Computer Architecture and Parallel Processing”, McGraw-Hill International Edition, 2000.
2. Sima D, Fountain T and Kacsuk P, ”Advanced Computer Architectures: A Design Space Approach”, Addison Wesley, 2000.

**Web References:**

1. https://onlinelibrary.wiley.com/doi/full/10.1002/9780470050118.ecse071
2. https://onlinelibrary.wiley.com/doi/pdf/10.1002/0471478385.fmatter

**E-Text Books:**

1. Rajiv Chopra, Advanced Computer Architecture, S. Chand Publishing, 2008

**Outcomes:**

1. Evaluate performance of different architectures with respect to various parameters
2. Analyze performance of different ILP techniques
3. Identify cache and memory related issues in multi-processors

# ROBOTIC TECHNOLOGY
## (Elective – V)

| M.Tech III Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES305** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. Design / Simulate a robot which meets kinematic requirements.
II. Apply localization and mapping aspects of mobile robotics.
III. Demonstrate self-learning capability.

| UNIT-I | INTRODUCTION | Classes:10 |
|---|---|---|

Robot anatomy-Definition, law of robotics, History and Terminology of Robotics-Accuracy and repeatability of Robotics-Simple problems, Specifications of Robot-Speed of Robot-Robot joints and links-Robot classifications-Architecture of robotic systems-Robot Drive systems Hydraulic, Pneumatic and Electric system.

| UNIT-II | END EFFECTORS AND ROBOT CONTROLS | Classes:10 |
|---|---|---|

Mechanical grippers-Slider crank mechanism, Screw type, Rotary actuators, cam type-Magnetic grippers-Vacuum grippers-Air operated grippers-Gripper force analysis-Gripper design-Simple problems-Robot controls-Point to point control, Continuous path control, Intelligent robot-Control system for robot joint-Control actions-Feedback devices-Encoder, Resolver, LVDT-Motion Interpolations-Adaptive control.

| UNIT-III | ROBOT TRANSFORMATIONS AND SENSORS | Classes:10 |
|---|---|---|

Robot kinematics-Types- 2D, 3D Transformation-Scaling, Rotation, Translation-Homogeneous coordinates, multiple transformation-Simple problems. Sensors in robot – Touch sensors-Tactile sensor – Proximity and range sensors – Robotic vision sensor-Force sensor-Light sensors, Pressure sensors.

| UNIT-IV | ROBOT CELL DESIGN AND APPLICATIONS | Classes:10 |
|---|---|---|

Robot work cell design and control-Sequence control, Operator interface, Safety monitoring devices in Robot-Mobile robot working principle, actuation using MATLAB, NXT Software Introductions-Robot applications, Material handling, Machine loading and unloading, assembly, Inspection, Welding, Spray painting and undersea robot.

| UNIT-V | MICRO/NANO ROBOTICS SYSTEM | Classes:10 |
|---|---|---|

Micro/Nanorobotics system overview-Scaling effect-Top down and bottom up approach-Actuators of Micro/Nano robotics system-Nanorobot communication techniques-Fabrication of micro/nano grippers-Wall climbing micro robot working principles-Biomimetic robot-Swarm robot-Nanorobot in
targeted drug delivery system.

**Text Books:**


1. S.R. Deb, Robotics Technology and flexible automation, Tata McGraw-Hill Education., 2009
2. Mikell P Groover& Nicholas G Odrey, Mitchel Weiss, Roger N Nagel, AshishDutta,

Industrial Robotics, Technology programming and Applications, McGraw Hill, 2012

**Reference Books:**

1. Richard D. Klafter, Thomas .A, ChriElewski, Michael Negin, Robotics Engineering an Integrated Approach, Phi Learning., 2009.
2. Francis N. Nagy, AndrasSiegler, Engineering foundation of Robotics, Prentice Hall Inc., 1987.

**Web References:**

1. https://en.wikipedia.org/wiki/Robotics
2. https://www.springer.com/in/book/9781852339531

**E-Text Books:**

1. P.A. Janaki Raman, Robotics and Image Processing an Introduction, Tata McGraw Hill Publishing company Ltd., 1995.
2. Carl D. Crane and Joseph Duffy, Kinematic Analysis of Robot manipulators, Cambridge University press, 2008.

**Outcomes:**

1. Identify a Robot for a specific application.
2. Interface various Servo and hardware components with Controller based projects.
3. Identify parameters required to be controlled in a Robot.

# EMBEDDED WIRELESS SENSOR NETWORKS
## (Elective – V)

| M.Tech III Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES306** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 4 | - | - | 4 | 40 | 60 | 100 |
| **Contact Classes:50** | **Tutorial Classes: -** | **Practical Classes: Nil** | | | **Total Classes:50** | | | |

**OBJECTIVES:**

**The course should enable the students to :**

I. To review the architecture of WSN.
II. To study the various protocols layers of WSN.
III. To study the establishment of WSN infrastructure.

| UNIT-I | INTRODUCTION | Classes:10 |
|---|---|---|

Characteristic requirements for WSN - Challenges for WSNs – WSN vs Adhoc Networks - Sensor node architecture – Commercially available sensor nodes –Imote, IRIS, Mica Mote, EYES nodes, BTnodes, TelosB, Sunspot -Physical layer and transceiver design considerations in WSNs, Energy usage profile, Choice of modulation scheme, Dynamic modulation scaling, Antenna considerations.

| UNIT-II | MEDIUM ACCESS CONTROL PROTOCOLS | Classes:10 |
|---|---|---|

Fundamentals of MAC protocols - Low duty cycle protocols and wakeup concepts – Contention based protocols - Schedule-based protocols - SMAC - BMAC - Traffic-adaptive medium access protocol (TRAMA) - The IEEE 802.15.4 MAC protocol.

| UNIT-III | ROUTING AND DATA GATHERING PROTOCOLS | Classes:10 |
|---|---|---|

Routing Challenges and Design Issues in Wireless Sensor Networks, Flooding and gossiping – Data centric Routing – SPIN – Directed Diffusion – Energy aware routing - Gradient-based routing - Rumor Routing – COUGAR – ACQUIRE – Hierarchical Routing - LEACH, PEGASIS – Location Based Routing – GF, GAF, GEAR, GPSR – Real Time routing Protocols – TEEN, APTEEN, SPEED, RAP - Data aggregation - data aggregation operations - Aggregate Queries in Sensor Networks - Aggregation Techniques – TAG, Tiny DB.

| UNIT-IV | EMBEDDED OPERATING SYSTEMS | Classes:10 |
|---|---|---|

Operating Systems for Wireless Sensor Networks – Introduction - Operating System Design Issues - Examples of Operating Systems – TinyOS – Mate – MagnetOS – MANTIS - OSPM - EYES OS – SenOS – EMERALDS – PicOS – Introduction to Tiny OS – NesC – Interfaces and Modules- Configurations and Wiring - Generic Components -Programming in Tiny OS using NesC, Emulator TOSSIM

| UNIT-V | APPLICATIONS OF WSN | Classes:10 |
|---|---|---|

WSN Applications - Home Control – Building Automation - Industrial Automation - Medical Applications - Reconfigurable Sensor Networks -Highway Monitoring - Military Applications - Civil and Environmental Engineering Applications - Wildfire Instrumentation - Habitat Monitoring - Nanoscopic Sensor Applications – Case Study: IEEE 802.15.4 LR-WPANs Standard - Target detection and tracking - Contour/edge detection - Field sampling.

**Text Books:**

1. C. S. Raghavendra, K.M. Sivalingam and T. Zanti," Wireless Sensor Networks",

Springer Verlag, Sep. 2006.
2. E. H. Callaway, Jr. Auerbach," Wireless Sensor Networks: Architectures and Protocols", Aug. 2003.

**Reference Books:**

1. K. SohrabyMinoli and T. Zanti," Wireless Sensor Networks: Technology, Protocols, and Applications", John Wiley and Sons, March 2007.
2. H. Karl, and A. Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley andSons, October 2007.

**Web References:**

1. https://pdfs.semanticscholar.org/921c/9c904a79f91b85a4b086cb446c4d33911c3c.pdf
2. http://www.eecg.toronto.edu/~jayar/pubs/brown/survey.pdf

**E-Text Books:**

1. A. ArockiaBazil Raj, FPGA-Based Embedded System Developer's Guide, and Applications, CRC Press, 2018.
2. Christian De Schryver, FPGA Based Accelerators for Financial Applications, Springer, 2016.

**Outcomes:**

1. Students will be introduced to some existing applications of wireless sensor actuator networks
2. Students will be introduced to elements of distributed computing and network protocol design and will learn to apply these principles in the context of wireless sensor networks
3. Students will learn the various hardware, software platforms that exist for sensor networks
4. Students will get an overview of the various network level protocols for MAC, routing, time
   synchronization, aggregation, consensus and distributed tracking
5. Students will read and present seminal papers on various issues in sensor networks, opening a path to research in this area
6. Students will understand what research problems sensor networks pose in disciplines such as signal processing, wireless communications and even control systems

## PROJECT WORK PHASE – I

| M.Tech III Semester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES307** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 0 | 0 | 20 | 10 | Grade | | |
| **Contact Classes:-** | **Tutorial Classes: -** | **Practical Classes: 40** | | | | **Total Classes:40** | | |

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ concerned department.

- **Registration of Project work**: A candidate is permitted to register for the project work phase-I after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Semesters).
- An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor/ Guide and one Internal senior expert shall monitor the progress of the project work.
- The work on the project work phase-I shall be initiated in the III semester and continued in the final semester. The candidate can submit Project work phase-I dissertation with the approval of I.D.C. after 18 weeks from the date of registration at the earliest from the date of registration for the project work phase-I.
- The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.
- Three copies of the Dissertation certified in the prescribed form by the supervisor and HOD shall be submitted to the HOD.
- The semester end examination for project work phase-I done during III Semester, shall be conducted by a Project Review Committee (PRC). The evaluation of project work shall be conducted at the end of the III Semester.
- The PRC comprises of an External examiner appointed by the Principal, Head of the Department and Project Guide/Supervisor to adjudicate the dissertation. The PRC shall jointly evaluate candidates work and award grades as given below.

| S.No | Description | Grade | Grade Point (GP) Assigned |
|---|---|---|---|
| 1 | Very Good | Grade A | 10 |
| 2 | Good | Grade B | 9 |
| 3 | Satisfactory | Grade C | 8 |
| 4 | Not satisfactory | Grade D | 0 |

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the dissertation.

## PROJECT WORK PHASE – II

| M.Tech IVSemester: EMBEDDED SYSTEM | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course code** | **Category** | **Hours/week** | | | **Credits** | **Maximum Marks** | | |
| **18ES401** | **Core** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **TOTAL** |
| | | 0 | 0 | 32 | 16 | Grade | | |
| **Contact Classes:-** | **Tutorial Classes: -** | **Practical Classes: 60** | | | | **Total Classes:60** | | |

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ concerned department.

- **Registration of Project work**: A candidate is permitted to register for the project work phase-I after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Semesters)
- An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor/ Guide and one Internal senior expert shall monitor the progress of the project work.
- The work on the project work phase-II shall be initiated in the IV semester. The candidate can submit Project work phase-II dissertation with the approval of I.D.C. after 18 weeks from the date of registration at the earliest from the date of registration for the project work phase-I.

- The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.
- Three copies of the Dissertation certified in the prescribed form by the supervisor and HOD shall be submitted to the HOD.
- The semester end examination for project work phase-I done during III Semester, shall be conducted by a Project Review Committee (PRC). The evaluation of project work shall be conducted at the end of the IV Semester.
- The PRC comprises of an External examiner appointed by the Principal, Head of the Department and Project Guide/Supervisor to adjudicate the dissertation. The PRC shall jointly evaluate candidates work and award grades as given below

| S.No | Description | Grade | Grade Point (GP) Assigned |
|---|---|---|---|
| 1 | Very Good | Grade A | 10 |
| 2 | Good | Grade B | 9 |
| 3 | Satisfactory | Grade C | 8 |
| 4 | Not satisfactory | Grade D | 0 |

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the dissertation.