ACADEMIC REGULATIONS

M.Tech Programmes

Regulation: R16

Applicable for the students admitted from the Academic year 2016-17 onwards

ASCET
AUDISANKARA Originating the Bright Careers

AUDISANKARA
COLLEGE OF ENGINEERING & TECHNOLOGY
An Autonomous Institute Affiliated to JNTUA, Ananthapuram & Accredited by NAAC with 'A' Grade

NH5 Bypass Road, Gudur, SPSR Nellore (Dt.)

www.audisankara.ac.in

REGULATIONS FOR M. TECH TWO YEAR REGULAR COURSES

R 1.0 Eligibility for Admission:

The admissions for category A and B seats shall be as per the guidelines of APSCHE in consonance with government reservation policy.

a) Under Category A: 70% of the seats are filled based on GATE/PGCET ranks.

b) Under Category B: 30% seats are filled on merit basis as per guidelines of APSCHE.

R 2.0 Semester wise Course Beak-up:

Sem	Theory	Lab	Total Credits
1st	6	2+ Technical Seminar	24
2nd	6	2+ Term Paper + Comprehensive Vive	26
3rd	7	Internship + Project Work	4 + 0
4th	4	Project Work	20
Total	23	5+Internship+ Project Work	74

R 2.1 Course wise break-up for the total credits:

Total Theory Courses : 23 @ 3 credits each = 69
Total Laboratory Courses : 5 @ 2 credits each = 15
Technical Seminar : 1 @ 2 credits = 2
Term Paper : 1 @ 2 credits = 2
Internship : 1 @ 2 credits = 2
Compre. Vive-Voce : 1 @ 2 credits = 2
Project work : 1 @ 20 credits =20

R 3.0 Division of marks for Internal and External assessment:

Course	Marks of Continuous Assessment	Marks of External Assessment	Maximum Marks
Theory	40	60	100
Labs	25	50	75
Term Paper	25	50	75
Comprehensive Viva-Voce	--	75	75
Internship	25	50	75
Project work	Grade	Grade	

R 4.0 Evaluation Methodology:

R 4.1 Theory Course:

Each theory course will be evaluated for a total of 100 marks, consisting of 40 marks for Continuous assessment and 60 marks for semester end examination. Following is the scheme for continuous assessment:

Scheme for Continuous Assessment:

Assessment Component	Marks	Schedule	Final Marks
Assignment Test#1 (AT#1)	5	After and on Unit#1	80% of first best SE + 20% of second best SE (30M) + AT#1 (5M) + AT#2 (5M)
Sessional Exam#1 (SE#1)	30	At the end of Unit#1 & 2	
Assignment Test#2 (AT#2)	5	After and on Unit#3	
Sessional Exam#2 (SE#2)	30	At the end of Unit#3 & 4	

4..1 (a) Scheme for SE Marks:

Two Sessional examinations (SE) each for 30 marks with the duration of 90 minutes each will be conducted for every theory course in a semester. The SE marks shall be awarded giving a weightage of 80% in the SE in which the student scores more marks and 20% in the remaining SE.

4.1 (b) Scheme for Assignment Test Marks:

Assignment test#1 shall be conducted for 5M at the end of Unit#1 covering the syllabus of unit#1. Assignment test#2 shall be conducted for 5M at the end of Unit#3 covering the syllabus of unit#3. Questions for Assignment test shall address the topics covered/ extension of the covered topics/Case Studies.

R 4.2 Laboratory Course:

a) Each lab will be evaluated for a total of 75 marks consisting of 25 marks for continuous assessment and 50 marks for semester end lab examination. Out of 25 marks of internal assessment, continuous lab assessment will be done for 15 marks for the day to day performance and 10 marks for the final internal lab assessment. The semester end lab examination for 50 marks shall be conducted by two Examiners, one of them being laboratory class Teacher as internal examiner and an external examiner nominated by the Principal from the panel of experts recommended by HOD.

R 4.3 Technical Seminar

Technical Seminar shall be conducted in 1st semester. The distribution of internal marks for component of Technical seminar is given below:

Table 5: Distribution of Marks for component of Technical seminar

S. No.	Criterion	Marks
1	Seminar Report & Subject content	20
2	Seminar presentation & Viva – Voce Exam	30

A Technical Seminar shall have two components, one chosen by the student from the course work as an extension and approved by the faculty supervisor. The other component is suggested by the supervisor and can be a reproduction of the concept in any standard research paper or an extension of concept from earlier course work. A hard copy of the information on seminar topic in the form of a report is to be submitted for evaluation along with presentation. The presentation of the seminar topics shall be made before a committee consisting of Head of the department, seminar supervisor and a senior faculty member. Each Technical Seminar shall be evaluated for 100 marks. Technical Seminar component-I for 50 marks and component-II for 50 marks making total 100 marks. (**Distribution of marks for 50:** 10 marks for report, 10 marks for subject content, 20 marks for presentation and 10 marks for queries).

R 5.3 Term Paper

The Term Paper is a self study report and shall be carried during 2nd semester along with other lab courses. Every student will take up this term paper individually and submit a report. The scope of the term paper could be an exhaustive literature review choosing any engineering concept with reference to a standard research papers or an extension of the concept of earlier course work in consultation with the term paper supervisor. The term paper reports submitted by the individual students during the second semester will be evaluated for a total of 75 marks consisting of 25 marks for internal assessment and 50 marks for semester end examination. Internal assessment shall be done by the term paper supervisor. Semester end examination for 50 marks shall be conducted by two examiners, one of them being term paper supervisor as internal examiner and an external Examiner nominated by the Principal from the panel of experts recommended by HOD.

R 5.4 Comprehensive Viva-Voce

All the students shall face a Comprehensive viva-voce covering the total courses of first and second semesters. The comprehensive viva-voce will be conducted along with 2nd semester lab examination for 75 marks by a committee consisting of Head of the Department, two senior faculty members nominated by the Head of the Department.

R 4.3 Internship

All the students shall undergo the summer internship during summer break after 2nd semester. The minimum internship period is eight weeks and the students have an option of choosing their own industry/area of interest, which may be related to their respective branch or any other service oriented task. A self study report for the internship shall be submitted and evaluated during the 3rd semester and will be evaluated for a total of 75 marks consisting of 25 marks for internal assessment and 50 marks for semester end examination. Internal assessment shall be done by the internship supervisor. Semester end examination for 50 marks shall be conducted by two examiners, one of them being internship supervisor as internal examiner and an external examiner nominated by the Principal from the panel of experts recommended by HOD.

R 4.6 Project Work

All the students shall take up a project work during 3rd and 4th semesters which carries a total of 20 credits. Every candidate shall be required to submit thesis or dissertation after completion of satisfactory work on a topic approved by the Project Review Committee.

a) A Project Review Committee (PRC) shall be constituted with the Dean (R&D), Head of the Department and one senior faculty member of the department apart from the Project Supervisor.
b) Registration of Project Work: A student is permitted to register for the project work in the beginning of the third semester after satisfying all the academic requirements.
c) A student has to submit the title, objective and plan of action of his project work in consultation with his project supervisor to the Project Review Committee (PRC) for its approval. After obtaining the approval of the Committee the student can initiate the Project work from the beginning of the third semester.
d) The project work initiated during the third semester shall be completed in duration of 10 months and its progress will be reviewed from time to time by the PRC.

e) Progress of the project work shall be reviewed in the 3rd semester tor two times for satisfactory performance of the student for zero credits. 20 credits shall be awarded based on the successful submission and approval of thesis at the end of the 4th semester.

f) On the completion of the project work the candidate shall submit the draft copy of thesis to the Head of the Department for the approval of PRC and shall make an oral presentation.

g) After the final approval by PRC, four copies of the Project Thesis certified by the supervisor shall be submitted to the Department.

h) Students are allowed to submit the project work/ thesis if s/he clears all the first and second semester courses.

i) The thesis shall be evaluated by one examiner selected by the Principal/Chief Controller of examinations from a panel of 5 examiners, who are eminent in the field and nominated by the concerned guide and Head of the department.

j) The following weightage are given for the continuous assessment as well as for the final evaluation of the project work:

i) Weightage for Supervisor evaluation	-	40 %
ii) Weightage for PRC evaluation	-	10%
iii) Weightage for External evaluation	-	50%

R5.0 Attendance Requirements:

a) It is desirable for a candidate to put on 100% attendance in all the subjects. However, a candidate shall be permitted to appear for the semester end examination provided s/he maintains a minimum of 75% overall attendance in the semester.

b) The shortage of attendance on medical grounds can be condoned to an extent of 10% provided a medical certificate is submitted to the Head of the Department when the candidate reports back to the classes immediately after the leave. Certificates submitted afterwards shall not be entertained. Condonation fee as fixed by the college for those who put on attendance between ≥ 65% and <75% shall be charged before the end examinations. Attendance may also be condoned as per the State Government rules for those who participate in sports, co-curricular and extra-curricular activities provided their attendance is in the minimum prescribed limits for the purpose and recommended by the concerned authority.

c) In case of the students having over all attendance less than 65% after condonation shall be declared detained and has to repeat semester again.

R 6.0 Promotion Policies:

a) A student shall be promoted to subsequent semester only if s/he fulfills the attendance requirement. In case a student fails to fulfill the attendance requirement, s/he has to repeat the semester in the next academic year.

b) A Student will be promoted from 2nd semester to 3rd semester if s/he fulfills the academic requirements and earning of minimum of 50% credits up to 2nd semester.

R 6.1 Scheme for the award of Grade

a) A student shall be deemed to have satisfied the minimum academic requirements and earn the credits for each theory course, if s/he secures

   i. Not less than 40% marks for each theory course in the semester end exam, and

   ii. A minimum of 40% marks for each theory course considering both internal and semester end examination.

   i. A student shall be deemed to have satisfied the minimum academic requirements and earn the credits for each Lab/ Technical Seminar/Term Paper/Comprehensive Viva/Internship/Project, if s/he secures not less than 50% marks for each Lab/ Term Paper/Mini Project/ Project course in the semester end exam,
   and

   ii. A minimum of 50% marks for each Lab/ Technical Seminar/Term Paper/Comprehensive Viva/Internship/Project course considering both internal and semester end examination.

R 6.2 Graduation requirements:

The following academic requirements shall be met for the award of the MCA. Degree.

a) Student shall register and acquire minimum attendance in all courses and secure 74 credits. However, the CGPA obtained for the best 71 credits shall be considered for the award of Grade/Class/Division.

b) A student of a regular program who fails to earn 91 credits within four consecutive academic years from the year of his/her admission with a minimum CGPA of 4.0 shall forfeit his/her degree and his/her admission stands cancelled.

R 6.3 Award of Degree:

a) Classification of degree will be as follows:

1. CGPA ≥ 7.5 : First Class with Distinction
2. CGPA ≥6.5 and < 7.5 : Degree with First Class
3. CGPA ≥5.5 and < 6.5 : Degree with Second Class
4. CGPA ≥4.0 and < 5.5 : Degree with Pass Class

b) Degree with Distinction will be awarded to those students who clear all the subjects in single attempt and secure a CGPA ≥ 8.0 during his/her regular course of study.

c) In case a student takes more than one attempt in clearing a course, the final marks secured shall be indicated by * mark in the marks memo.

All the candidates who register for the semester end examination will be issued memorandum of grades by the Institute. Apart from the semester wise marks memos, the institute will issue the provisional certificate subject to the fulfillment of all the academic requirements.

R7.0 Re-Admission Criteria:

A Candidate, who is detained in a year/semester due to lack of attendance/credits, has to obtain written permission from the Principal for readmission into the same semester after duly fulfilling all the required norms stipulated by the college in addition to paying the required fee.

R8.0 Conduct & Discipline:-

(a) Students shall conduct themselves within and outside the premises of the Institute in a descent and dignified manner befitting the students of Audisankara College of Engineering & Technology.

(b) As per the order of the Honorable Supreme Court of India, ragging in any form is considered a criminal offence and is totally banned. Any form of ragging will be severely dealt with.

(c) The following acts of omission and / or commission shall constitute gross violation of the code of conduct and are liable to invoke disciplinary measures with regard to ragging.

(i) Lack of courtesy and decorum; indecent behavior anywhere within or outside the college campus.

(ii) Damage of college property or distribution of alcoholic drinks or any kind of narcotics to fellow students / citizens.

(d) Possession, consumption or distribution of alcoholic drinks or any kind of narcotics or hallucinogenic drugs.

(e) Mutilation or unauthorized possession of library books.

(f) Noisy and unruly behavior, disturbing studies of fellow students.

(g) Hacking in computer systems (such as entering into other person's areas without prior permission, manipulation and / or damage of computer hardware and software or any other cyber crime etc.

(h) Usage of camera /cell phones in the campus.

(i) Plagiarism of any nature.

(j) Any other act of gross indiscipline as decided by the college academic council from time to time.

(k) Commensurate with the gravity of offense, the punishment may be reprimand, fine, expulsion from the institute/ hostel, debarring from examination, disallowing the use of certain facilities of the Institute, rustication for a specified period or even outright expulsion from the Institute, or even handing over the case to appropriate law enforcement authorities or the judiciary, as required by the circumstances.

(l) For an offence committed in (i) a hostel (ii) a department or in a class room and (iii) elsewhere, the chief Warden, the concern Head of the Department and the Principal respectively, shall have the authority to reprimand or impose fine.

(m) Cases of adoption of unfair means and/ or any malpractice in an examination shall be reported to the principal for taking appropriate corrective action.

(n) All cases of serious offence, possibly requiring punishment other than reprimand, shall be reported to the Academic council of the college.

(o) The Institute Level Standing Disciplinary Action Committee constituted by the academic council shall be the authority to investigate the details of the offence, and recommend disciplinary action based on the nature and extent of the offence committed.

(p) The Principal shall deal with any problem, which is not covered under these rules and regulations.

(q) **"Grievance and Redressal Committee" (General)** constituted by the Principal shall deal with all grievances pertaining to the academic / administrative / disciplinary matters.

(r) All the students must abide by the code and conduct rules prescribed by the college from time to time.

R9.0 Transitory Regulations:

A student, who is detained or discontinued in the year/semester, on readmission shall be required to do all the courses in the curriculum prescribed for such batch of students in which the student joins subsequently.

R9.1 A student who is following the JNTUA, Anantapur curriculum/R13 regulations, detained due to lack of credits/ attendance at the end of the any semester of any year, shall join the forthcoming autonomous/ R13 batch (es) (which ever applicable) after fulfilling the requirements. Such students will study all the courses prescribed for that batch, in which the student joins. The student has to clear all backlog subjects if any by appearing in the supplementary examinations of JNTUA/R13 for the award of degree. The class will be awarded based on the academic performance of a student. Such candidates will be considered on par with R13 stream and will be governed by the regulations applicable.

R9.2 A student who is following the JNTUA, Anantapur curriculum/R13, detained due to lack of credits/ attendance at the end of any semester, shall join the autonomous batch at the appropriate semester. Such candidates shall be required to pass in all the courses in the Programme prescribed by concerned BoS for such batch of students, to be eligible for the award of degree. However, exemption will be given in all those courses of the semester(s) of the batch, which the candidate joins now, which he had passed earlier. The student has to clear all his backlog subjects by appearing in the supplementary examinations, conducted by JNTUA, Anantapur and College (Autonomous Stream) for the Award of Degree. The class will be awarded based on the academic performance of a student in the JNTUA Pattern and academic regulations of JNTUA will be followed.

General:

a) s/he represents "she" and "he" both
b) Where the words 'he', 'him', 'his', occur, they imply 'she', 'her', 'hers' also.
c) The academic regulations should be read as a whole for the purpose of any interpretation.
d) In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman, Academic Council will be final.

The college may change or amend the academic regulations or syllabi from time to time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the institute.

Course Structure for M.Tech (VLSI) Regular Programme

Applicable for students admitted from 2016-17 Academic Year

M.Tech 1st Semester – VLSI

S.No	Code	Course	L	P	C
1	16VL1101	VLSI Technology and Design	3	0	3
2	16VL1102	CMOS Analog Integrated Circuit Design	3	0	3
3	16VL1103	CMOS Digital Integrated Circuit Design	3	0	3
4	16VL1104	Hardware Description Languages	3	0	3
5	16VL1105	Device Modeling	3	0	3
6	**ELECTIVE-I**				
	16VL1106	Embedded System Concepts	3	0	3
	16VL1107	Scripting language for VLSI Design Automation			
	16VL1108	ASIC Design			
7	16VL2109	CMOS Analog Integrated Circuit Design Lab	0	3	2
8	16VL2110	CMOS Digital Integrated Circuit Design Lab	0	3	2
9	16VL2111	Technical Seminar	2	0	2
		TOTAL	**20**	**6**	**24**

M.Tech 2nd Semester – VLSI

S.No	Code	Course	L	P	C
1	16VL1201	FPGA Architecture and Applications	3	0	3
2	16VL1202	Testing and Testability	3	0	3
3	16VL1203	Low Power VLSI Design	3	0	3
4	16VL1204	Algorithms for VLSI Design Automation	3	0	3
5	16VL1205	Hardware Software Co-Design	3	0	3
6	**ELECTIVE-II**				
	16VL1206	DSP Processors and Architectures	3	0	3
	16VL1207	RFIC Design			
	16VL1208	Real Time Operating Systems			
7	16VL2209	Mixed Signal Lab	0	3	2
8	16VL2210	Embedded Processing Lab	0	3	2
9	16VL2211	Term Paper	2	0	2
10	16VL2212	Comprehensive Viva-Voce	0	0	2
		TOTAL	**20**	**6**	**26**

M.Tech 3rd Semester – VLSI

S.No	Code	Course	L	P	C
1	16VL2301	Internship + Project Work	0	0	4
		TOTAL	**0**	**0**	**4**

M.Tech 4th Semester – VLSI

S.No	Code	Course	L	P	C
1	16VL2401	Project Work	0	0	20
		TOTAL	**0**	**0**	**20**

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 1st Semester –VLSI

L	T	P	C
3	0	0	3

16VL1101 VLSI TECHNOLOGY AND DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 To be aware about the trends in semiconductor technology, and how it impacts scaling and performance
2 To understand MOS transistor as a switch and its capacitance
3 learn Layout, Stick diagrams, Fabrication steps, Static and Switching characteristics of inverters
4 Design, built and debug complex combinational and sequential circuits based on an abstract functional specification.
5 Synthesis of digital VLSI systems from register-transfer or higher level descriptions in hardware design languages.
6 Student will be able to design digital systems using MOS circuits.

UNIT-I

Review of Microelectronics and Introduction to MOS Technologies: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

Basic Electrical Properties of MOS, CMOS & BICOMS Circuits: Ids -Vds Relationships, Threshold Voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, Zpu/Zpd, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT-II

Layout Design and Tools: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT-III

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

Sequential Systems: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT-IV

Floor Planning & Architecture Design: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

Introduction to CAD Systems (Algorithms) and Chip Design: Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

TEXT BOOKS:

1 K. Eshraghian et . al(3 authors), Essentials of VLSI Circuits and Systems, , PHI of India Ltd.,2005
2 Wayne Wolf, Modern VLSI Design, 3rd ed., Pearson Education,2005.

REFERENCE BOOKS:

1 N.H.E Weste, K.Eshraghian, Adison Wesley, Principals of CMOS Design, 2nd ed.,1993
2 Fabricius, Introduction to VLSI Design, MGH International Edition, 1990.
3 Baker, Li Boyce, CMOS Circuit Design, Layout and Simulation, PHI, 2004.

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AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 1st Semester –VLSI

L	T	P	C
3	0	0	3

16VL1102 CMOS ANALOG INTEGRATED CIRCUIT DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 Students will demonstrate the use of analog circuit analysis techniques to analyze the operation and behavior of various analog integrated circuits.
2 Students will demonstrate their knowledge by designing analog circuits
3 Design, simulation and synthesize analog circuits
4 Analyze the basic current mirrors
5 Analyze and design basic operational amplifiers
6 understand the concept of gain, power, and bandwidth

UNIT-I

MOS transistors- Modeling in linear, saturation and cutoff high frequency equivalent circuit.
Integrated Devices and Modeling and Current Mirror: Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load. Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors and Bipolar Gain Stages. Frequency Response.

UNIT-II

Operational Amplifier Design and Compensation: Two Stage CMOS Operational Amplifier. Feedback and Operational Amplifier Compensation. Advanced Current Mirror. Folded–Cascade Operational Amplifier, Current Mirror Operational Amplifier Fully Differential Operational Amplifier. Common Mode Feedback Circuits. Current Feedback Operational Amplifier. Comparator. Charge Injection Error. Latched Comparator and Bi-CMOS Comparators.
Sample and Hold Switched Capacitor Circuits-I: MOS, CMOS, Bi-CMOS Sample and Hold Circuits. Switched Capacitor Circuits: Basic Operation and Analysis. First Order and Biquard Filters.

UNIT-III

Sample and Hold Switched Capacitor Circuits-II: Charge Injection. Switched Capacitor Gain Circuit. Correlated. Double Sampling Techniques. Other Switched Capacitor Circuits.
Data Converters: Ideal D/A & A/D Converters. Quantization Noise. Performance Limitations. Nyquist Rate D/Converters: Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating ,Successive Approximation, Cyclic Flash Type, Two Step, Interpolating, Folding and Pipelined, A/D Converters.

UNIT-IV

Over Sampling Converters and Filters: Over Sampling With and Without Noise Shaping. Digital Decimation Filter. High Order Modulators. Band Pass Over Sampling Converter. Practical Considerations. Continuous Time Filters.

TEXT BOOKS:

1 D.A.John, Ken Martin, Analog Integrated Circuit Design", 1st ed., John Wiley, 1996.
2 Behzad Razavi, Design of Analog CMOS Integrated Circuit, Tata-Mc GrawHill, 1st ed.,2002.

REFERENCE BOOKS:

1 Philip Allen & Douglas Holberg, CMOS Analog Circuit Design, Oxford University Press, 3rd ed.,2011
2 GREGOLIAN &TEMES: Analog MOS Integrated Circuits, John Wiley, 1986.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 1st Semester –VLSI

L	T	P	C
3	0	0	3

16VL1103 CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 To study about CMOS inverters and its applications
2 To design low power CMOS circuits
3 To analyze the Bi-CMOS logic circuits
4 To study the layout design rules for designing the circuits
5 To study the static and dynamic characteristics of CMOS inverters
6 To analyze the ALU sub-system design

UNIT-I

CMOS inverters -static and dynamic characteristics.
Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

UNIT-II

Method of Logical Effort for Transistor Sizing -power consumption in CMOS gates- Low power CMOS design.
Arithmetic Circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

UNIT-III

Bipolar gate Design- BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.
Layout Design Rules: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT-IV

Subsystem Design Process: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

TEXT BOOKS:

1 Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, 2nd ed.,MGH,1999.
2 Jan M Rabaey, Digital Integrated Circuits-ADesign Perspective,2nd ed.Prentice Hall,2003.
3 Eugene D Fabricus, Introduction to VLSI Design, McGraw Hill International Edition, 1990.

REFERENCE BOOKS:

1 Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000.
2 Neil H E West and Kamran Eshranghian, Principles of CMOS VLSI Design: A System Perspective",2nd ed., Addision-Wesley,2002.
3 R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation,IEEE Press, 1998.
4 David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, 3rd ed., McGraw-Hill, 2004

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 1st Semester –VLSI

L	T	P	C
3	0	0	3

16VL1104 HARDWARE DESCRIPTION LANGUAGES

COURSE OUTCOMES:

At the end of the course students able to

1 Understand verilog program structures
2 understand gate level and switch level modeling
3 design various program descriptions
4 Design digital systems using simple and moderately complex systems using methodologies that are common for the implementation to reconfigurable logic devices.
5 Use typical design techniques for combinational circuits, asynchronous and synchronous state machines and busses.
6 Implement the process of synthesis and post-synthesis in the developed systems and verify their functioning once implemented in reconfigurable logic devices.

UNIT-I

Hardware Modeling with the Verilog HDL: Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

Logic System, Data Types and Operators for Modeling in Verilog HDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives – Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT-II

Behavioral Descriptions in Verilog HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

Synthesis of Combinational Logic: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares, Synthesis of Sequential Logic Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT-III

Synthesis of Language Constructs: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

Switch – Level Models in Verilog: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

UNIT-IV

Introduction to HDL: An Overview of Design Procedures used for System Design using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. Design Verification Tools. Examples using Commercial PC Based on VHDL Elements of VHDL Top Down Design with VHDL Subprograms. Controller Description VHDL Operators.

Behavioral Description of Hardware in HDL: Process Statement Assertion Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design. Differences between VHDL and Verilog.

TEXT BOOKS:

1 M.D.CILETTI, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice-Hall, 1999.
2 Z.NAWABI, VHDL Analysis and Modeling of Digital Systems, 2nd ed., McGraw Hill, 1998.

REFERENCE BOOKS:

1 M.G.ARNOLD, Verilog Digital – Computer Design, Prentice-Hall (PTR), 1999.
2 PERRY, VHDL, 3rd ed., McGraw Hill.

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M.Tech 1st Semester –VLSI

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16VL1105 Device Modeling

COURSE OUTCOMES:

At the end of the course students able to

1 Develop solution to overcome short channel issues
2 Develop compact models appropriate for industry
3 Analyze current distribution in the devices like transistors and MOS devices
4 Understand different types of spice modeling's
5 Understand different fabrication techniques
6 understand the Eber-Moll, Gunmel - Poon bipolar model

UNIT-I

Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures.

UNIT-II

Integrated Diodes: Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models.

Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model- dynamic model, Parasitic effects – SPICE model –Parameter extraction.

UNIT-III

Integrated MOS Transistor:NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4.

UNIT-IV

VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements.

Modeling of Hetero Junction Devices: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe.

TEXT BOOKS:

1 Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2 Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS:

1 Sze S. M, Physics of Semiconductor Devices, 2nd Edition, Mcgraw Hill, New York, 1981.
2 Tor A. Fijedly , Introduction to Device Modeling and Circuit Simulation, Wiley-Interscience, 1997
3 Ming-BO Lin, Introduction to VLSI Systems: A Logic, Circuit and System Perspective, CRC Press, 2011

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16VL1106 EMBEDDED SYSTEM CONCEPTS

COURSE OUTCOMES:

At the end of the course students able to

1 Describe the differences between the general computing system and the embedded system, also recognize the classification of embedded systems..
2 Design real time embedded systems using the concepts of RTOS.
3 To understand the processor and memory organization in an embedded system.
4 To learn the basic instruction set of ARM, SHARC processor and programming concepts.
5 To study devices and buses used in embedded system.
6 To understand the concept of Hardware- Software C0- Design in an Embedded System

UNIT-I

Introduction to Embedded Systems: An Embedded System, Processor in The System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System -On-Chip (SOC) and in VLSI Circuit.

Processor and Memory Organization: Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

UNIT-II

Devices and Buses for Device Networks: I/O Devices, Timer and Counting Devices, Serial Communication Using The "I^2C" , CAN, Profibus Foundation Field Bus. and Advanced I/O Buses Between the Network Multiple Devices, Host Systems or Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses.

Device Drivers and Interrupts Servicing Mechanism: Device Drivers, Parallel Port and Serial Port Device Drivers in a System, Device Drivers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

UNIT-III

Instruction Sets: Introduction, preliminaries, ARM processor, SHARC processor.

Programming Concepts and Embedded Programming in C, C++, VC++ and JAVA: Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

UNIT-IV

Hardware- Software C0- Design in an Embedded System: Embedded System Project Management, Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, use of Target Systems, use of Software Tools for Development of an Embedded System, use of Scopes and Logic Analysis for System, Hardware Tests. Issues in Embedded System Design.

TEXT BOOKS:

1 Rajkamal, Embedded systems: Architecture, Programming and Design, TMH, 2008.
2 wayne wolf, Computers as a component: principles of embedded computing system design.

REFERENCE BOOKS:

1 Arnold S Berger, Embedded System Design, 1st ed., CMP Books, 2001.
2 An embedded software primer by David Simon, 1st Indian Reprint, PEA, 2001.
3 Steve Heath, Embedded systems design: Real world design , Newton Mass USA, 2002.
4 Hayt, Data communication.

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16VL1107 SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION

COURSE OUTCOMES:

At the end of the course students able to

1 Learn concepts of PERL, CGI, VB Script, Java Script.
2 Analyze PERL Pattern Matching, Data Structures, Modules, Objects, Tied Variables.
3 Understand the Inter process Communication Threads
4 Identify the various Portable Functions and Extensive Exercises for Programming in PERL .
5 Study of VB Script, Java Script with Programming Examples

UNIT-I

Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.

UNIT-II

Inter process Communication Threads, Compilation & Line Interfacing.

UNIT-III

Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL .

UNIT-IV

Other Languages: Broad Details of CGI, VB Script, Java Script with Programming Examples.

TEXT BOOKS:

1 Randal L, Schwartz Tom Phoenix, Learning PERL, 3rd ed., Oreilly Publications, 2000
2 Larry Wall, Tom Christiansen, John Orwant, Programming PERL, 3rd ed., Oreilly Publications 2000.
3 Tom Christiansen, Nathan Torkington, PERL Cookbook, 3rd ed., Oreilly Publications, 2000.

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16VL1108 ASIC DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 Demonstrate in-depth knowledge in ASIC Design Styles, ASICs Design Issues, ASICs Design Techniques, ASIC Construction.
2 Analyze the characteristics and Performance of ASICs and judge independently the best suited device for fabrication of smart devices for conducting research in ASIC design.
3 Solve problems of Design issues, simulation and Testing of ASICs.
4 Apply appropriate techniques, resources and tools to engineering activities for appropriate Solution to develop ASICs.
5 Understand different FPGA Partitioning methods

UNIT-I

ASIC Design Styles: Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs.

ASICS – Programmable Logic Devices: Overview – PAL –based PLDs: Structures; PAL Characteristics – FPGAs: Introduction, selected families – design outline.

UNIT-II

ASICS –Design Issues: Design methodologies and design tools – design for testability – economies.

ACISS Characteristics and Performance: design styles, gate arrays, standard cell -based ASICs, Mixed mode and analogue ASICs.

UNIT-III

ASICS-Design Techniques: Overview- Design flow and methodology-Hardware description languages-simulation and checking-commercial design tools- FPGA Design tools: XILINX, ALTERA

Logic Synthesis, Simulation and Testing: Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation- automatic test pattern generation

UNIT-IV

ASIC Construction: Floor planning, placement and routing system partition.

FPGA Partitioning: Partitioning Methods-Floor Planning- Placement-Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

TEXT BOOKS:

1 L.J.Herbst, Integrated Circuit Engineering, OXFORD SCIENCE Publications, 1996.

REFERENCE BOOKS:

1 M.J.S.Smith, Application - Specific integrated circuits, Addison-Wesley Longman Inc ,1997.

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16VL2109 CMOS ANALOG INTEGRATED CIRCUIT DESIGN LAB

COURSE OUTCOMES:

At the end of the course students able to

1 Model NMOS inverter
2 Design and simulate CMOS inverter with W/L ratio
3 Produce layout of CMOS inverter and extract parasitic elements
4 Familiarize the design of current source mirror using BJT and MOS
5 Study the design of differential amplifier and to extract the design outcome.

LIST OF EXPERIMENTS

1. **NMOS Inverter:** Depletion and Enhancement Mode Circuit Simulation and Adjustment of Vh VLSI Vm parameters for NMOS inverter.
2. **CMOS Inverter:** Circuit Simulation, adjustment of W / L ratio of P & N channel MOS transistor for symmetrical drive output and loading consideration. Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners).Layout of CMOS Inverter, Extraction of parasitic and back annotation and related modifications in circuit parameters and layout.
3. **Current Source / Mirror:** Circuit simulation of current Mirror using BJT and MOS(Simple, Wilson and Wilder configurations) study and modifications to improve power and load regulation. Layout of CMOS Current Mirror.
4. **8 Bit shift register cell:** Building of cell Library of logic gates and flip flops and building of 8 bit shift register from the same. Optimization of the same from layout and power considerations.
5. **Differential Amplifier:**

Study of specifications of Differential amplifier and Design considerations. Study of input loading and biasing techniques.

REQUIRED SOFTWARE TOOLS: Mentor Graphic tools / Cadence tools/ Synopsys's tools/Microwind. (180 nm Technology and Above)

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16VL2110 CMOS DIGITAL INTEGRATED CIRCUIT DESIGN LAB

COURSE OUTCOMES:

At the end of the course students able to

1 apply theory and practice for designing digital logic circuits and logic system designs
2 Familiarize with the VHDL using Xilinx
3 Verify the design logic of combinational and sequential circuit
4 Simulate timing analysis and to calculate critical path time
5 Programming on FPGA for different digital logic circuits

1. Digital Circuits Description using Verilog and VHDL.
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits.
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

REQUIRED SOFTWARE TOOLS:

1 Mentor Graphic tools / Cadance tools/ Synophysis tools. (180 nm Technology and Above)
2 Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

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16VL2111 TECHNICAL SEMINAR

COURSE OUTCOMES:

At the end of the course students able to

1 Analyze and develop a thought process for presentation
2 Improve his language and communication skills
3 Be conversant with the latest developments in power systems

A Technical Seminar shall have two components, one chosen by the student from the course work as an extension and approved by the faculty supervisor. The other component is suggested by the supervisor and can be a reproduction of the concept in any standard research paper or an extension of concept from earlier course work. A hard copy of the information on seminar topic in the form of a report is to be submitted for evaluation along with presentation. The presentation of the seminar topics shall be made before a committee consisting of Head of the department, seminar supervisor and a senior faculty member. Each Technical Seminar shall be evaluated for 100 marks. Technical Seminar component-I for 50 marks and component-II for 50 marks making total 100 marks. (**Distribution of marks for 50:** 10 marks for report, 10 marks for subject content, 20 marks for presentation and 10 marks for queries).

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16VL1201 FPGA ARCHITECTURE AND APPLICATIONS

COURSE OUTCOMES:

At the end of the course students able to

1 Able to gain the knowledge about PLDs, FPGA Design & architectures.
2 Students should be able to understand different types of FSM's
3 Different FSM techniques like ASM and One-hot Design method
4 Understand the various frontend design tools and implementation process.
5 Analyze System level Design and their application for Combinational and Sequential Circuits.

UNIT-I

Programmable Logic: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

FPGA: Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

UNIT-II

Case Studies: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

Finite State Machines(FSM): Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

UNIT-III

Realization of State Machine: Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

FSM Architectures and Systems Level Design: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

UNIT-IV

Digital Front End Digital Design Tools for FPGAS & ASICS: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

TEXT BOOKS:

1 P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall, 1994.
2 S.Trimberger , Field Programmable Gate Array Technology, Kluwer Academic Publications,1994.

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16VL1202 TESTING AND TESTABILITY

COURSE OUTCOMES:

At the end of the course students able to

1 To study the modeling of digital circuits
2 To analyze the fault detection and fault correction
3 To analyze the fault modeling
4 To design the testing of single stuck faults
5 To design the built in self test(BIST) circuits
6 To study about Memory BIST(MBIST) and embedded core testing

UNIT-I

Introduction to Test and Design for Testability (DFT) Fundamentals: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

Fault Modeling: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

UNIT-II

Testing for Single Stuck Faults (SSF): Automated Test Pattern Generation (ATPG/ATG) For Ssfs In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models. Vector Simulation – ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

Design for Testability: Testability Trade-Offs, Techniques. Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design. Board Level and System Level DFT Approaches. Boundary Scans Standards. Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT-III

Built – in Self – Test (BIST): BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT-IV

Memory BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

Brief Ideas on Embedded Core Testing: Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

TEXT BOOKS:

1 Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, 1st ed., Jaico Publishing House, 2001.

REFERENCE BOOKS:

1 Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall, 1999.
2 Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, 1998.

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16VL1203 LOW POWER VLSI DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 Trends in semiconductor technology, and how it impacts scaling and performance.
2 Low-power design concepts and voltage-frequency scaling.
3 Understand different isolation techniques in BICMOS technology
4 design deep-submicron silicon technologies, high performance simulation models likewise hspice, pspice.
5 Apply in practice technology-level, circuit-level, and system-level power optimization techniques.
6 Design different high performance digital circuits, optimization theme, performance theme.

UNIT-I

Low Power Design, an Over View: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS Processes: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT-II

Low-Voltage/Low Power CMOS/ BICMOS Processes: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT-III

CMOS and Bi-CMOS Logic Gates: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

Low- Voltage Low Power Logic Circuits: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation

UNIT-IV

Low Power Latches and Filip Flops: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

Special Techniques: Power Reduction in Clock Networks, CMOS Floating Node,Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

TEXT BOOKS:

1 1. Yeo Rofail/ Gohl(3 Authors), "CMOS/BiCMOS ULSI low voltage, low power", Pearson Education Asia, 1st Indian reprint,2002.
2 Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP, 2002.

REFERENCE BOOKS:

1 Douglas A.Pucknell & Kamran Eshraghian, Basic VLSI Design, 3rd ed., PHI, 2005.
2 J.Rabaey, Digital Integrated circuits, PHI,1996
3 Sung-mo Kang and Yusuf Leblebici, CMOS Digital ICs, 3rd ed., TMH 2003.
4 IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia

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16VL1204 ALGORITHMS FOR VLSI DESIGN AUTOMATION

COURSE OUTCOMES:

At the end of the course students able to

1 Ability to model automation of VLSI design.
2 Ability to apply optimization techniques to the process of VLSI design.
3 Understand the layout compaction, modeling and simulation.
4 Learn the concepts of logic and high level synthesis and verification.
5 Analyze the physical design Automation of FPGA and MCM'S

UNIT-I

Preliminaries: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

General Purpose Methods for Combinational Optimization: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT-II

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

Modelling and Simulation: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT-III

Logic Synthesis and Verification: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

High – Level Synthesis: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT-IV

Physical Design Automation of FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

Physical Design Automation of MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin, Distribution and routing, Routing and Programmable MCM's.

TEXT BOOKS:

1 S.H.Gerez, Algorithms for VLSI Design Automation, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999
2 Naveed Sherwani, Algorithms for VLSI Physical Design Automation ,3rd ed., Springer International edition, 2005

REFERENCE BOOKS:

1 Hill & Peterson, Computer Aided Logical Design with Emphasis on VLSI, Wiley, 1993.
2 Wayne Wolf, Modern VLSI Design Systems on silicon, 2nd ed., Pearson Education Asia, 1998

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16VL1205 HARDWARE SOFTWARE CO-DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 Analyze hardware-software co-design problems for systems with moderate complexity.
2 Apply hardware-software co-design methods and techniques to practical problems.
3 Designing hardware-software co-design solutions through SoPC and similar technologies.
4 Applying different levels of abstractions and provide models for verification of the architecture and functionality for embedded co-design solutions.
5 Evaluate and compare quality solutions compared to for example: performance, cost, security, power consumption and size.
6 Partition and design space exploration with LYCOS

UNIT-I

Co-Design Issues: Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware- software partitioning distributed system co-synthesis.

UNIT-II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III

Compilation Techniques and Tools for Embedded Processor:

Architectures: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT-IV

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS:

1 Jorgen Staunstrup, Wayne Wolf, Hardware / software co- design Principles and Practice, Springer,2009.
2 Hardware / software co- design Principles and Practice, Kluwer Academic Publishers , 2002.

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16VL1206 DSP PROCESSORS AND ARCHITECTURES

COURSE OUTCOMES:

At the end of the course students able to

1 Comprehends the knowledge & concepts of digital signal processing techniques.
2 Learn the DSP programming tools and use them for applications
3 Students will be able to use the DSP processors TMS 320C 54XX for implementation of DSP algorithms & its interfacing techniques with various I/O peripherals.
4 Students will be able to use MATLAB DSP toolbox for analysis & design of DSP.
5 Acquire knowledge of DSP computational building blocks and knows how to Achieve speed in DSP architecture or processor.
6 Learn the architecture details and instruction sets of fixed and floating point DSPs

UNIT-I

Introduction to Digital Signal Processing:

Introduction, Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

Computational Accuracy in DSP Implementations:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II

Architectures for Programmable DSP Devices:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Execution Control and Pipelining:

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT-III

Programmable Digital Signal Processors:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and

Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

Implementations of Basic DSP Algorithms:

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters,Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT-IV

Implementation of FFT Algorithms:

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

Interfacing Memory and I/O Peripherals to Programmable DSP Devices:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1 Avtar Singh and S. Srinivasan, Digital Signal Processing, Thomson Publications, 2004.
2 Lapsleyetal, DSP Processor Fundamentals, Architectures & Features, S.Chand & Co, 2000.

REFERENCE BOOKS:

1 B. Venkata Ramani, M. Bhaskar, Digital Signal Processors, Architecture, Programming and Applications, 4th ed. Reprint,TMH,2008.
2 Jonatha Stein, Digital Signal Processing ,1st ed., John Wiley, 2005

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 2nd Semester –VLSI

L	T	P	C
3	0	0	3

16VL1207 RFIC DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 Learn basic concepts of RF and wireless technology
2 Understand the various RF design concepts
3 Analyze techniques and wireless standards
4 Learn architecture of transreceiver
5 Study different types of power amplifiers, considerations and linearization techniques

UNIT-I

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology.

BASIC CONCEPTS IN RF DESIGN: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT-II

MULTIPLE ACCESS: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards.

TRANSCEIVER ARCHITECTURES: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

UNIT-III

AMPLIFIERS, MIXERS AND OSCILLATORS: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

UNIT-IV

POWER AMPLIFIERS: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques.

TEXT BOOKS:

1 BehzadRazavi, RF Microelectronics Prentice Hall of India, 2001.
2 Thomas H. Lee, The Design of CMOS Radio Integrated Circuits, Cambridge University Press.

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L	T	P	C
3	0	0	3

16VL1208 REAL TIME OPERATING SYSTEMS

COURSE OUTCOMES:

At the end of the course students able to

1 To distinguish a real-time system from other systems.
2 To identify the functions of operating system.
3 To evaluate the need for real-time operating system.
4 To implement the real-time operating system principles.
5 To analyze the case studies like VX works, RT Linux.
6 To understand the fault tolerance techniques in real time operating systems.

UNIT-I

Introduction to UNIX: Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

Real Time Systems: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

UNIT-II

Approaches to Real Time Scheduling: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

Operating Systems: Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

UNIT-III

Fault Tolerance Techniques: Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

Case Studies – VX Works: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

UNIT-IV

RT Linux: Process Management, Scheduling, Interrupt Management, and Synchronization

TEXT BOOKS:

1 Richard Stevens, Advanced Unix Programming, 2nd ed., Addison-Wesley, 2005.
2 Jane W.S. Liu, Real Time Systems, 1st ed., Pearson Education, 2000
3 C.M.Krishna, KANG G. Shin, Real Time Systems, McGraw.Hill, 1997

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M.Tech 2nd Semester –VLSI	**L**	**T**	**P**	**C**
	0	**0**	**3**	**2**

16VL1209 **MIXED SIGNAL LAB**

COURSE OUTCOMES:

At the end of the course students able to

1 Familiarize the Analog Circuits Simulation using Spice
2 Design of Layout Vs Schematic.
3 Generate Net List Extraction
4 Implements Design Rule Checks for various analog and digital designs

LIST OF EXPERIMENTS

1. Analog Circuits Simulation using Spice.
2. Mixed Signal Simulation Using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
6. Net List Extraction.
7. Design Rule Checks.

Required Software Tools:

Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
Xilinx 9.1i and Above for FPGA/CPLDS.

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M.Tech 2nd Semester –VLSI	**L**	**T**	**P**	**C**
	0	**0**	**3**	**2**

16VL2210 **EMBEDDED PROCESSING LAB**

COURSE OUTCOMES:

At the end of the course students able to

1 Familiarize with the ALP and C program using RTOS 8051 kits.
2 Dump the programs into the microcontroller kits using flash magic software.
3 Study ARM evaluation board and familiarize with basic programming concepts.
4 write programs to interface various I/O devices with PIC micro controllers

LIST OF EXPERIMENTS:

1. Study of different addressing modes Using 89C51/PIC microcontroller.
2. General purpose input output (GP10) ports using 89C51/PIC microcontroller
3. Keyboard Interface using embedded micro controller.
4. LED and LCD Interface using 89C51/PIC Micro controller.
5. RTD and Thermocouple Interface using embedded micro controller
6. ADC and DAC Interface using embedded micro controller.
7. I^2C RTC interface using embedded micro controller
8. Alarm clock using embedded micro controller.
9. Testing RTOS Environment and System Programming using KEIL software.
10. Flash controller programming - Data flash with erase , verify, fusing through ATMEL/INTEL tools.

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M.Tech 2nd Semester –VLSI	L	T	P	C
	2	0	0	2

16VL2211 TERM PAPER

The Term Paper is a precursor to the project work done in the 2nd year M.Tech Programme. The paper may be of 8-10 (A4 size) in length and follows the standard IEEE/Technical Journal Format.

The Term Paper helps to supplement the second year Project Work of the M.Tech students. It helps to identify their Research area/topic and complete the groundwork and preliminary research required for it comfortably. It trains the students to make use of Research Tools and Material available both in print and digital formats.

Based on the topic, a hypothesis is to be made by the student, under the supervision of the guide. The student is then required to collect literature and support information for his / her term paper from Standard Reference Books, Journals, and Magazines - both printed and online. Each student should refer to a minimum of 6 reference sources related to the topic. The student also presents his/her paper with the help of Power Point slides / OHP.

The Term Paper contains: The Aim and Objective of the study, The need for Rationale behind the study, Identify the work already done in the field, Hypothesis and Discussion, Conclusion Appendix with support data (Illustrations, Tables, Graphs, etc.).

Page Limit: minimum of eight pages.

Date of evaluation: During the Lab Internal Exam.

Method of Evaluation: Total 50 marks

1. Day to day work - 10 marks
2. Term Paper Report - 20 marks
3. Seminar - 20 marks

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M.Tech 2nd Semester –VLSI

L	T	P	C
0	0	0	2

16VL2212 COMPREHENSIVE VIVA-VOCE

COURSE OUTCOMES:

At the end of the course students able to

1 Test the learning and understanding during the course of under graduate program.
2 Face interview both at the academic and the industrial sector.

All the students shall face a Comprehensive viva-voce covering the total courses of first and second semesters. The comprehensive viva-voce will be conducted along with 2nd semester lab examination for 75 marks by a committee consisting of Head of the Department, two senior faculty members nominated by the Head of the Department

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M.Tech 3rd Semester –VLSI	**L**	**T**	**P**	**C**
	0	**0**	**0**	**4**

16VL2301 INTERNSHIP + PROJECT WORK

COURSE OUTCOMES:

At the end of the course students able to

1 develop awareness, understanding and capacity in the specific roles and responsibilities in an industry
2 develop and refinement of technical and professional skills

All the students shall undergo the summer internship during summer break after 2nd semester. The minimum internship period is eight weeks and the students have an option of choosing their own industry/area of interest, which may be related to their respective branch or any other service oriented task. A self study report for the internship shall be submitted and evaluated during the 3rd semester and will be evaluated for a total of 75 marks consisting of 25 marks for internal assessment and 50 marks for semester end examination. Internal assessment shall be done by the internship supervisor. Semester end examination for 50 marks shall be conducted by two examiners, one of them being internship supervisor as internal examiner and an external examiner nominated by the Principal from the panel of experts recommended by HOD

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(AUTONOMOUS)

M.Tech 4th Semester –VLSI	**L**	**T**	**P**	**C**
	0	**0**	**0**	**20**

16VL2401 **PROJECT WORK**

COURSE OUTCOMES:

At the end of the course students able to

1 Identify a problem of current relevance to society
2 Formulate the problem and identify suitable modeling paradigm.
3 Analyze the problem and identify the solution methodology

Students are required to take up a project work, in which the student can choose any specific problem of Industry or Industry based project work. Alternatively it can be secondary source based or Field based project work. Before the commencement of the project work each student is required to submit a synopsis indicating the objectives, Methodology, Framework for analysis, Action plan with milestones in order to have clarity for the subsequent work. The project should have an internal faculty as guide. The student can initiate the project work in the penultimate semester of the course