ACADEMIC REGULATIONS

M.Tech Programmes

Regulation: R16

Applicable for the students admitted from the Academic year 2016-17 onwards

ASCET
AUDISANKARA Originating the Bright Careers

AUDISANKARA
COLLEGE OF ENGINEERING & TECHNOLOGY
An Autonomous Institute Affiliated to JNTUA, Ananthapuram & Accredited by NAAC with 'A' Grade

NH5 Bypass Road, Gudur, SPSR Nellore (Dt.)

www.audisankara.ac.in

REGULATIONS FOR M. TECH TWO YEAR REGULAR COURSES

R 1.0 Eligibility for Admission:

The admissions for category A and B seats shall be as per the guidelines of APSCHE in consonance with government reservation policy.

a) Under Category A: 70% of the seats are filled based on GATE/PGCET ranks.

b) Under Category B: 30% seats are filled on merit basis as per guidelines of APSCHE.

R 2.0 Semester wise Course Beak-up:

Sem	Theory	Lab	Total Credits
1st	6	2+ Technical Seminar	24
2nd	6	2+ Term Paper + Comprehensive Vive	26
3rd	7	Internship + Project Work	4 + 0
4th	4	Project Work	20
Total	23	5+Internship+ Project Work	74

R 2.1 Course wise break-up for the total credits:

Total Theory Courses : 23 @ 3 credits each = 69
Total Laboratory Courses : 5 @ 2 credits each = 15
Technical Seminar : 1 @ 2 credits = 2
Term Paper : 1 @ 2 credits = 2
Internship : 1 @ 2 credits = 2
Compre. Vive-Voce : 1 @ 2 credits = 2
Project work : 1 @ 20 credits =20

R 3.0 Division of marks for Internal and External assessment:

Course	Marks of Continuous Assessment	Marks of External Assessment	Maximum Marks
Theory	40	60	100
Labs	25	50	75
Term Paper	25	50	75
Comprehensive Viva-Voce	--	75	75
Internship	25	50	75
Project work	Grade	Grade	

R 4.0 Evaluation Methodology:

R 4.1 Theory Course:

Each theory course will be evaluated for a total of 100 marks, consisting of 40 marks for Continuous assessment and 60 marks for semester end examination. Following is the scheme for continuous assessment:

Scheme for Continuous Assessment:

Assessment Component	Marks	Schedule	Final Marks
Assignment Test#1 (AT#1)	5	After and on Unit#1	80% of first best SE + 20% of second best SE (30M) + AT#1 (5M) + AT#2 (5M)
Sessional Exam#1 (SE#1)	30	At the end of Unit#1 & 2	
Assignment Test#2 (AT#2)	5	After and on Unit#3	
Sessional Exam#2 (SE#2)	30	At the end of Unit#3 & 4	

4..1 (a) Scheme for SE Marks:

Two Sessional examinations (SE) each for 30 marks with the duration of 90 minutes each will be conducted for every theory course in a semester. The SE marks shall be awarded giving a weightage of 80% in the SE in which the student scores more marks and 20% in the remaining SE.

4.1 (b) Scheme for Assignment Test Marks:

Assignment test#1 shall be conducted for 5M at the end of Unit#1 covering the syllabus of unit#1. Assignment test#2 shall be conducted for 5M at the end of Unit#3 covering the syllabus of unit#3. Questions for Assignment test shall address the topics covered/ extension of the covered topics/Case Studies.

R 4.2 Laboratory Course:

a) Each lab will be evaluated for a total of 75 marks consisting of 25 marks for continuous assessment and 50 marks for semester end lab examination. Out of 25 marks of internal assessment, continuous lab assessment will be done for 15 marks for the day to day performance and 10 marks for the final internal lab assessment. The semester end lab examination for 50 marks shall be conducted by two Examiners, one of them being laboratory class Teacher as internal examiner and an external examiner nominated by the Principal from the panel of experts recommended by HOD.

R 4.3 Technical Seminar

Technical Seminar shall be conducted in 1st semester. The distribution of internal marks for component of Technical seminar is given below:

Table 5: Distribution of Marks for component of Technical seminar

S. No.	Criterion	Marks
1	Seminar Report & Subject content	20
2	Seminar presentation & Viva – Voce Exam	30

A Technical Seminar shall have two components, one chosen by the student from the course work as an extension and approved by the faculty supervisor. The other component is suggested by the supervisor and can be a reproduction of the concept in any standard research paper or an extension of concept from earlier course work. A hard copy of the information on seminar topic in the form of a report is to be submitted for evaluation along with presentation. The presentation of the seminar topics shall be made before a committee consisting of Head of the department, seminar supervisor and a senior faculty member. Each Technical Seminar shall be evaluated for 100 marks. Technical Seminar component-I for 50 marks and component-II for 50 marks making total 100 marks. (**Distribution of marks for 50:** 10 marks for report, 10 marks for subject content, 20 marks for presentation and 10 marks for queries).

R 5.3 Term Paper

The Term Paper is a self study report and shall be carried during 2nd semester along with other lab courses. Every student will take up this term paper individually and submit a report. The scope of the term paper could be an exhaustive literature review choosing any engineering concept with reference to a standard research papers or an extension of the concept of earlier course work in consultation with the term paper supervisor. The term paper reports submitted by the individual students during the second semester will be evaluated for a total of 75 marks consisting of 25 marks for internal assessment and 50 marks for semester end examination. Internal assessment shall be done by the term paper supervisor. Semester end examination for 50 marks shall be conducted by two examiners, one of them being term paper supervisor as internal examiner and an external Examiner nominated by the Principal from the panel of experts recommended by HOD.

R 5.4 Comprehensive Viva-Voce

All the students shall face a Comprehensive viva-voce covering the total courses of first and second semesters. The comprehensive viva-voce will be conducted along with 2nd semester lab examination for 75 marks by a committee consisting of Head of the Department, two senior faculty members nominated by the Head of the Department.

R 4.3 Internship

All the students shall undergo the summer internship during summer break after 2nd semester. The minimum internship period is eight weeks and the students have an option of choosing their own industry/area of interest, which may be related to their respective branch or any other service oriented task. A self study report for the internship shall be submitted and evaluated during the 3rd semester and will be evaluated for a total of 75 marks consisting of 25 marks for internal assessment and 50 marks for semester end examination. Internal assessment shall be done by the internship supervisor. Semester end examination for 50 marks shall be conducted by two examiners, one of them being internship supervisor as internal examiner and an external examiner nominated by the Principal from the panel of experts recommended by HOD.

R 4.6 Project Work

All the students shall take up a project work during 3rd and 4th semesters which carries a total of 20 credits. Every candidate shall be required to submit thesis or dissertation after completion of satisfactory work on a topic approved by the Project Review Committee.

a) A Project Review Committee (PRC) shall be constituted with the Dean (R&D), Head of the Department and one senior faculty member of the department apart from the Project Supervisor.
b) Registration of Project Work: A student is permitted to register for the project work in the beginning of the third semester after satisfying all the academic requirements.
c) A student has to submit the title, objective and plan of action of his project work in consultation with his project supervisor to the Project Review Committee (PRC) for its approval. After obtaining the approval of the Committee the student can initiate the Project work from the beginning of the third semester.
d) The project work initiated during the third semester shall be completed in duration of 10 months and its progress will be reviewed from time to time by the PRC.

e) Progress of the project work shall be reviewed in the 3rd semester tor two times for satisfactory performance of the student for zero credits. 20 credits shall be awarded based on the successful submission and approval of thesis at the end of the 4th semester.

f) On the completion of the project work the candidate shall submit the draft copy of thesis to the Head of the Department for the approval of PRC and shall make an oral presentation.

g) After the final approval by PRC, four copies of the Project Thesis certified by the supervisor shall be submitted to the Department.

h) Students are allowed to submit the project work/ thesis if s/he clears all the first and second semester courses.

i) The thesis shall be evaluated by one examiner selected by the Principal/Chief Controller of examinations from a panel of 5 examiners, who are eminent in the field and nominated by the concerned guide and Head of the department.

j) The following weightage are given for the continuous assessment as well as for the final evaluation of the project work:

i) Weightage for Supervisor evaluation	-	40 %
ii) Weightage for PRC evaluation	-	10%
iii) Weightage for External evaluation	-	50%

R5.0 Attendance Requirements:

a) It is desirable for a candidate to put on 100% attendance in all the subjects. However, a candidate shall be permitted to appear for the semester end examination provided s/he maintains a minimum of 75% overall attendance in the semester.

b) The shortage of attendance on medical grounds can be condoned to an extent of 10% provided a medical certificate is submitted to the Head of the Department when the candidate reports back to the classes immediately after the leave. Certificates submitted afterwards shall not be entertained. Condonation fee as fixed by the college for those who put on attendance between ≥ 65% and <75% shall be charged before the end examinations. Attendance may also be condoned as per the State Government rules for those who participate in sports, co-curricular and extra-curricular activities provided their attendance is in the minimum prescribed limits for the purpose and recommended by the concerned authority.

c) In case of the students having over all attendance less than 65% after condonation shall be declared detained and has to repeat semester again.

R 6.0 Promotion Policies:

a) A student shall be promoted to subsequent semester only if s/he fulfills the attendance requirement. In case a student fails to fulfill the attendance requirement, s/he has to repeat the semester in the next academic year.

b) A Student will be promoted from 2nd semester to 3rd semester if s/he fulfills the academic requirements and earning of minimum of 50% credits up to 2nd semester.

R 6.1 Scheme for the award of Grade

a) A student shall be deemed to have satisfied the minimum academic requirements and earn the credits for each theory course, if s/he secures

   i. Not less than 40% marks for each theory course in the semester end exam, and

   ii. A minimum of 40% marks for each theory course considering both internal and semester end examination.

   i. A student shall be deemed to have satisfied the minimum academic requirements and earn the credits for each Lab/ Technical Seminar/Term Paper/Comprehensive Viva/Internship/Project, if s/he secures not less than 50% marks for each Lab/ Term Paper/Mini Project/ Project course in the semester end exam,
   and

   ii. A minimum of 50% marks for each Lab/ Technical Seminar/Term Paper/Comprehensive Viva/Internship/Project course considering both internal and semester end examination.

R 6.2 Graduation requirements:

The following academic requirements shall be met for the award of the MCA. Degree.

a) Student shall register and acquire minimum attendance in all courses and secure 74 credits. However, the CGPA obtained for the best 71 credits shall be considered for the award of Grade/Class/Division.

b) A student of a regular program who fails to earn 91 credits within four consecutive academic years from the year of his/her admission with a minimum CGPA of 4.0 shall forfeit his/her degree and his/her admission stands cancelled.

R 6.3 Award of Degree:

a) Classification of degree will be as follows:

1. CGPA ≥ 7.5 : First Class with Distinction
2. CGPA ≥6.5 and < 7.5 : Degree with First Class
3. CGPA ≥5.5 and < 6.5 : Degree with Second Class
4. CGPA ≥4.0 and < 5.5 : Degree with Pass Class

b) Degree with Distinction will be awarded to those students who clear all the subjects in single attempt and secure a CGPA ≥ 8.0 during his/her regular course of study.

c) In case a student takes more than one attempt in clearing a course, the final marks secured shall be indicated by * mark in the marks memo.

All the candidates who register for the semester end examination will be issued memorandum of grades by the Institute. Apart from the semester wise marks memos, the institute will issue the provisional certificate subject to the fulfillment of all the academic requirements.

R7.0 Re-Admission Criteria:

A Candidate, who is detained in a year/semester due to lack of attendance/credits, has to obtain written permission from the Principal for readmission into the same semester after duly fulfilling all the required norms stipulated by the college in addition to paying the required fee.

R8.0 Conduct & Discipline:-

(a) Students shall conduct themselves within and outside the premises of the Institute in a descent and dignified manner befitting the students of Audisankara College of Engineering & Technology.

(b) As per the order of the Honorable Supreme Court of India, ragging in any form is considered a criminal offence and is totally banned. Any form of ragging will be severely dealt with.

(c) The following acts of omission and / or commission shall constitute gross violation of the code of conduct and are liable to invoke disciplinary measures with regard to ragging.

(i) Lack of courtesy and decorum; indecent behavior anywhere within or outside the college campus.

(ii) Damage of college property or distribution of alcoholic drinks or any kind of narcotics to fellow students / citizens.

(d) Possession, consumption or distribution of alcoholic drinks or any kind of narcotics or hallucinogenic drugs.

(e) Mutilation or unauthorized possession of library books.

(f) Noisy and unruly behavior, disturbing studies of fellow students.

(g) Hacking in computer systems (such as entering into other person's areas without prior permission, manipulation and / or damage of computer hardware and software or any other cyber crime etc.

(h) Usage of camera /cell phones in the campus.

(i) Plagiarism of any nature.

(j) Any other act of gross indiscipline as decided by the college academic council from time to time.

(k) Commensurate with the gravity of offense, the punishment may be reprimand, fine, expulsion from the institute/ hostel, debarring from examination, disallowing the use of certain facilities of the Institute, rustication for a specified period or even outright expulsion from the Institute, or even handing over the case to appropriate law enforcement authorities or the judiciary, as required by the circumstances.

(l) For an offence committed in (i) a hostel (ii) a department or in a class room and (iii) elsewhere, the chief Warden, the concern Head of the Department and the Principal respectively, shall have the authority to reprimand or impose fine.

(m) Cases of adoption of unfair means and/ or any malpractice in an examination shall be reported to the principal for taking appropriate corrective action.

(n) All cases of serious offence, possibly requiring punishment other than reprimand, shall be reported to the Academic council of the college.

(o) The Institute Level Standing Disciplinary Action Committee constituted by the academic council shall be the authority to investigate the details of the offence, and recommend disciplinary action based on the nature and extent of the offence committed.

(p) The Principal shall deal with any problem, which is not covered under these rules and regulations.

(q) **"Grievance and Redressal Committee" (General)** constituted by the Principal shall deal with all grievances pertaining to the academic / administrative / disciplinary matters.

(r) All the students must abide by the code and conduct rules prescribed by the college from time to time.

R9.0 Transitory Regulations:

A student, who is detained or discontinued in the year/semester, on readmission shall be required to do all the courses in the curriculum prescribed for such batch of students in which the student joins subsequently.

R9.1 A student who is following the JNTUA, Anantapur curriculum/R13 regulations, detained due to lack of credits/ attendance at the end of the any semester of any year, shall join the forthcoming autonomous/ R13 batch (es) (which ever applicable) after fulfilling the requirements. Such students will study all the courses prescribed for that batch, in which the student joins. The student has to clear all backlog subjects if any by appearing in the supplementary examinations of JNTUA/R13 for the award of degree. The class will be awarded based on the academic performance of a student. Such candidates will be considered on par with R13 stream and will be governed by the regulations applicable.

R9.2 A student who is following the JNTUA, Anantapur curriculum/R13, detained due to lack of credits/ attendance at the end of any semester, shall join the autonomous batch at the appropriate semester. Such candidates shall be required to pass in all the courses in the Programme prescribed by concerned BoS for such batch of students, to be eligible for the award of degree. However, exemption will be given in all those courses of the semester(s) of the batch, which the candidate joins now, which he had passed earlier. The student has to clear all his backlog subjects by appearing in the supplementary examinations, conducted by JNTUA, Anantapur and College (Autonomous Stream) for the Award of Degree. The class will be awarded based on the academic performance of a student in the JNTUA Pattern and academic regulations of JNTUA will be followed.

General:

a) s/he represents "she" and "he" both
b) Where the words 'he', 'him', 'his', occur, they imply 'she', 'her', 'hers' also.
c) The academic regulations should be read as a whole for the purpose of any interpretation.
d) In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman, Academic Council will be final.

The college may change or amend the academic regulations or syllabi from time to time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the institute.

Course Structure for M.Tech (Embedded Systems) Regular Programme

Applicable for students admitted from 2016-17 Academic Year

M.Tech 1st Semester – Embedded Systems

S.No	Code	Course	L	P	C
1	16ES1101	Microcontrollers for Embedded System Design	3	0	3
2	16ES1102	Advanced Computer Architecture	3	0	3
3	16ES1103	Embedded System Concepts	3	0	3
4	16ES1104	VLSI Technology and Design	3	0	3
5	16ES1105	DSP Processors and Architectures	3	0	3
6	**ELECTIVE-I**				
	16ES1106	CMOS Digital Integrated Circuit Design	3	0	3
	16ES1107	Embedded Computing			
	16ES1108	Advanced Operating Systems			
7	16ES2109	Microcontrollers and Interfacing Lab	0	3	2
8	16ES2110	IC System Design Lab	0	3	2
9	16ES2111	Technical Seminar	2	0	2
		TOTAL	**20**	**6**	**24**

M.Tech 2nd Semester – Embedded Systems

S.No	Code	Course	L	P	C
1	16ES1201	FPGA Architecture and Applications	3	0	3
2	16ES1202	Real Time Operating Systems	3	0	3
3	16ES1203	System on Chip Architecture	3	0	3
4	16ES1204	Cryptography and Network Security	3	0	3
5	16ES1205	Hardware Software Co-Design	3	0	3
6	**ELECTIVE-II**				
	16ES1206	Robotic Technology	3	0	3
	16ES1207	Embedded Networks			
	16ES1208	Software Defines Radio			
7	16ES1209	RTOS and FPGA Lab	0	3	2
8	16ES2210	Advanced Embedded Systems Lab	0	3	2
9	16ES2211	Term Paper	2	0	2
10	16ES2212	Comprehensive Viva-Voce	0	0	2
		TOTAL	**20**	**6**	**26**

M.Tech 3rd Semester – Embedded Systems

S.No	Code	Course	L	P	C
1	16ES2301	Internship + Project Work	0	0	4
		TOTAL	**0**	**0**	**4**

M.Tech 4th Semester – Embedded Systems

S.No	Code	Course	L	P	C
1	16ES2401	Project Work	0	0	20
		TOTAL	**0**	**0**	**20**

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 1st Semester –ES

L	T	P	C
3	0	0	3

16ES1101 MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 To understand outline architecture of ARM7 microcontroller including basics of pipelines, registers, exception modes, etc.
2 To learn ARM7 instruction set covering branching, data processing instructions, swap instruction, THUMB instruction set and others.
3 To learn Software development flow and working with projects.
4 To give an overview of system peripherals which cover bus structure, memory map, register programming.
5 To set up and customize a microcontroller development environment.
6 To understand the basic concepts of memory management in ARM microcontroller

UNIT-I

ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families

UNIT-II

ARM Programming Model – I: Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT-III

ARM Programming Model – II: Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT-IV

ARM Programming: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1 Andrew N. Sloss, Dominic Symes, Chris Wright, ARM Systems Developer's Guides-Designing & Optimizing System Software, Elsevier, 2008.

REFERENCE BOOKS:

1 Jonathan W. Valvano – Brookes / Cole, Embedded Microcomputer Systems, Real Time Interfacing,Thomas Learning, 1999.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 1st Semester –ES

L	T	P	C
3	0	0	3

16ES1102 ADVANCED COMPUTER ARCHITECTURE

COURSE OUTCOMES:

At the end of the course students able to

1. Understand the concepts of cost- measuring and reporting performance quantitative principles of computer design.
2. Describe modern architectures such as RISC, Super Scalar, VLIW
3. Describe the operation of virtual memory.
4. Describe the principles of computer design.
5. Classify instruction set architectures

UNIT-I

Fundamentals of Computer Design: Technology trends, cost- measuring and reporting performance quantitative principles of computer design.

Instruction Set Principles and Examples: Classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set- instructions for control flow- encoding an instruction set.-the role of compiler

UNIT-II

Instruction Level Parallelism (ILP): Overc oming data hazards, reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP

ILP Software Approach: Compiler Techniques, Static Branch Protection, VLIW Approach, H.W support for more ILP at compile time- H.W verses S.W solutions

UNIT-III

Memory Hierarchy Design: Cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

Multiprocessors and Thread Level Parallelism: Symmetric shared memory architectures, distributed shared memory, Synchronization, multi threading.

UNIT-IV

Storage Systems: Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

Inter Connection Networks and Clusters: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster

TEXT BOOKS:

1 1. John. Hennessy & David A. Patterson Morgan Kufmann, *Computer Architecture- A quantitative approach*, 5th ed., Elsevier, 2011.

REFERENCE BOOKS:

1 Kai Hwang and A. Briggs, *Computer Architecture and parallel Processing*, International Edition McGraw-Hill, 1984.
2 Dezso Sima, Terence Fountain, Peter Kacsuk, Advanced Computer Architectures, Pearson.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 1st Semester –ES	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

16ES1103 EMBEDDED SYSTEM CONCEPTS

COURSE OUTCOMES:

At the end of the course students able to

1 Describe the differences between the general computing system and the embedded system, also recognize the classification of embedded systems..
2 Design real time embedded systems using the concepts of RTOS.
3 To understand the processor and memory organization in an embedded system.
4 To learn the basic instruction set of ARM, SHARC processor and programming concepts.
5 To study devices and buses used in embedded system.
6 To understand the concept of Hardware- Software C0- Design in an Embedded System

UNIT-I

Introduction to Embedded Systems: An Embedded System, Processor in The System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System -On-Chip (SOC) and in VLSI Circuit.

Processor and Memory Organization: Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

UNIT-II

Devices and Buses for Device Networks: I/O Devices, Timer and Counting Devices, Serial Communication Using The "I^2C" , CAN, Profibus Foundation Field Bus. and Advanced I/O Buses Between the Network Multiple Devices, Host Systems or Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses.

Device Drivers and Interrupts Servicing Mechanism: Device Drivers, Parallel Port and Serial Port Device Drivers in a System, Device Drivers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

UNIT-III

Instruction Sets: Introduction, preliminaries, ARM processor, SHARC processor.

Programming Concepts and Embedded Programming in C, C++, VC++ and JAVA: Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

UNIT-IV

Hardware- Software C0- Design in an Embedded System: Embedded System Project Management, Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, use of Target Systems, use of Software Tools for Development of an Embedded System, use of Scopes and Logic Analysis for System, Hardware Tests. Issues in Embedded System Design.

TEXT BOOKS:

1 Rajkamal, Embedded systems: Architecture, Programming and Design, TMH, 2008.
2 wayne wolf, Computers as a component: principles of embedded computing system design.

REFERENCE BOOKS:

1 Arnold S Berger, Embedded System Design, 1st ed., CMP Books, 2001.
2 An embedded software primer by David Simon, 1st Indian Reprint, PEA, 2001.
3 Steve Heath, Embedded systems design: Real world design , Newton Mass USA, 2002.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 1st Semester –ES

L	T	P	C
3	0	0	3

16ES1104 VLSI TECHNOLOGY AND DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 To be aware about the trends in semiconductor technology, and how it impacts scaling and performance
2 To understand MOS transistor as a switch and its capacitance
3 learn Layout, Stick diagrams, Fabrication steps, Static and Switching characteristics of inverters
4 Design, built and debug complex combinational and sequential circuits based on an abstract functional specification.
5 Synthesis of digital VLSI systems from register-transfer or higher level descriptions in hardware design languages.
6 Student will be able to design digital systems using MOS circuits.

UNIT-I

Review of Microelectronics and Introduction to MOS Technologies: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

Basic Electrical Properties of MOS, CMOS & BICOMS Circuits: Ids -Vds Relationships, Threshold Voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, Zpu/Zpd, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT-II

Layout Design and Tools: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT-III

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

Sequential Systems: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT-IV

Floor Planning & Architecture Design: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

Introduction to CAD Systems (Algorithms) and Chip Design: Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

TEXT BOOKS:

1 Essentials of VLSI Circuits and Systems, K. Eshraghian et . al(3 authors), PHI of India Ltd.,2005
2 Wayne Wolf, Modern VLSI Design, 3rd ed., Pearson Education,2005.

REFERENCE BOOKS:

1 N.H.E Weste, K.Eshraghian, Adison Wesley, Principals of CMOS Design, 2nd ed.,1993.
2 Fabricius, Introduction to VLSI Design, MGH International Edition, 1990.
3 Baker, Li Boyce, CMOS Circuit Design, Layout and Simulation, PHI, 2004.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 1st Semester –ES

L	T	P	C
3	0	0	3

16ES1105 DSP PROCESSORS AND ARCHITECTURES

COURSE OUTCOMES:

At the end of the course students able to

1 Comprehends the knowledge & concepts of digital signal processing techniques.
2 Learn the DSP programming tools and use them for applications
3 Students will be able to use the DSP processors TMS 320C 54XX for implementation of DSP algorithms & its interfacing techniques with various I/O peripherals.
4 Students will be able to use MATLAB DSP toolbox for analysis & design of DSP.
5 Acquire knowledge of DSP computational building blocks and knows how to Achieve speed in DSP architecture or processor.
6 Learn the architecture details and instruction sets of fixed and floating point DSPs

UNIT-I

Introduction to Digital Signal Processing Introduction, Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

Computational Accuracy in DSP Implementations

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II

Architectures for Programmable DSP Devices

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Execution Control and Pipelining

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT-III

Programmable Digital Signal Processors

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of

TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

Implementations of Basic DSP

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT-IV

Implementation of FFT Algorithms

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

Interfacing Memory and I/O Peripherals to Programmable DSP Devices

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1 Avtar Singh and S. Srinivasan, Digital Signal Processing, Thomson Publications, 2004.
2 Lapsleyetal, DSP Processor Fundamentals, Architectures & Features, S.Chand & Co, 2000.

REFERENCE BOOKS:

1 B. Venkata Ramani, M. Bhaskar, Digital Signal Processors, Architecture, Programming and Applications, 4th ed. Reprint,TMH,2008.
2 Jonatha Stein, Digital Signal Processing ,1st ed., John Wiley, 2005.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 1st Semester –ES

L	T	P	C
3	0	0	3

16ES1106 CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 To study about CMOS inverters and its applications
2 To design low power CMOS circuits
3 To analyze the Bi-CMOS logic circuits
4 To study the layout design rules for designing the circuits
5 To study the static and dynamic characteristics of CMOS inverters
6 To analyze the ALU sub-system design

UNIT-I

CMOS inverters -static and dynamic characteristics.
Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

UNIT-II

Method of Logical Effort for Transistor Sizing -power consumption in CMOS gates- Low power CMOS design.
Arithmetic Circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

UNIT-III

Bipolar gate Design- Bi-CMOS logic - static and dynamic behaviour -Delay and power consumption in Bi-CMOS Logic.
Layout Design Rules: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT-IV

Subsystem Design Process: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

TEXT BOOKS:

1 Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, 2nd ed., MGH,1999.
2 Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, 2nd ed.,Prentice Hall, 2003.
3 Eugene D Fabricus, Introduction to VLSI Design, McGraw Hill International Edition, 1990.

REFERENCE BOOKS:

1 Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000.
2 Neil H E West and Kamran Eshranghian, Principles of CMOS VLSI Design: A System Perspective",2nd ed., Addision-Wesley,2002.
3 David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, 3rd ed., McGraw-Hill, 2004.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 1st Semester –ES

L	T	P	C
3	0	0	3

16ES1107 EMBEDDED COMPUTING

COURSE OUTCOMES:

At the end of the course students able to

1 Able to learn programming on LINUX platform.
2 Understand the Operating System Overview
3 Learn Software Development Tools
4 Analyze the interfacing modules and openCV for machine vision
5 Get knowledge on TCP/IP,UDP and other networking basics.
6 Understand IA32 instruction set

UNIT-I

Programming on Linux Platform: System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. Operating System Overview: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue

UNIT-II

Introduction to Software Development Tools: GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

UNIT-III

Interfacing Modules: Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

UNIT-IV

Networking Basics: Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.
IA32 Instruction Set: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:

1 Peter Barry and Patrick Crowley, Modern Embedded Computing, 1st Ed., Elsevier/Morgan Kaufmann,2012.
2 Michael K. Johnson, Erik W. Troan, Linux Application Development, Adission Wesley, 1998.
3 Kip R. Irvine, Assembly Language for x86 Processors.
4 Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS:

1 Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2 The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3 UNIX Network Programming by W. Richard Stevens

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 1st Semester –ES

L	T	P	C
3	0	0	3

16ES1108 ADVANCED OPERATING SYSTEMS

COURSE OUTCOMES:

At the end of the course students able to

1 Master functions, structures and history of operating systems
2 Understand the concepts of UNIX and LINUX
3 Learn process creation and termination
4 study the inter process communication and client server example
5 Learn the goals of distributed system and design issues
6 understand the algorithms of synchronization in distributed systems

UNIT-I

Introduction to Operating Systems: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System.

UNIT-II

Introduction to UNIX and LINUX: Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations.

UNIT-III

System Calls: System calls and related file structures, Input / Output, Process creation & termination. Inter Process Communication Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT-IV

Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues. Communication in Distributed Systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

Synchronization in Distributed Systems: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:

1 Maurice J. Bach, The design of the UNIX Operating Systems, PHI, 1986.
2 Andrew. S. Tanenbaum, Distributed Operating System, PHI, 1994.
3 Richard Peterson, The Complete reference LINUX, 4th Ed., McGraw – Hill.
4 Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.

REFERENCE BOOKS:

1 Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
2 Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
3 UNIX User Guide – Ritchie & Yates.
4 UNIX Network Programming - W.Richard Stevens, 1998, PHI.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 1st Semester –ES

L	T	P	C
0	0	3	2

16ES2109 MICROCONTROLLERS AND INTERFACING LAB

COURSE OUTCOMES:

At the end of the course students able to

1 familiarize with the assembly level programming using keil software
2 Design circuits for various applications using microcontrollers
3 An in-depth knowledge of applying the concepts on real- time applications

LIST OF EXPERIMENTS:

Assembly:

1. Write a program to a) Clear the Register and b) Add 3 to Register Ten Times and Place the Result into Memory Use the Indirect Instructions to Perform Looping.

Programming in C:

2. A Door Sensor is connected to RB1 Pin and a Buzzer is connected to RB7. Write a Program to monitor Door Sensor and when it Open, Sounds the Buzzer by sending a Square Wave of few Hundred Hz Frequency to it.
3. Write a Program to Toggle all the Bits of PORT B parts continuously with a 250ns Delay.
4. Stepper Motor Control using Microcontroller.

Use Microcontrollers for the following Experiments.

Interfacing:

5. Elevator Interface.
6. Key Board Interface.
7. LED Interface.
8. Temperature Sensor.
9. SORT RTO'S on to 89c51 Board.
10. Sample the Signal using ADC and Reconstruct by using DAC.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 1st Semester –ES

L	T	P	C
0	0	3	2

16ES2110 **IC SYSTEM DESIGN LAB**

COURSE OUTCOMES:

At the end of the course students able to

1 apply theory and practice for designing digital logic circuits and logic system designs
2 Familiarize with the VHDL using Xilinx
3 Verify the design logic of combinational and sequential circuit
4 Simulate timing analysis and to calculate critical path time
5 Programming on FPGA for different digital logic circuits

LIST OF EXPERIMENTS:

1. Design and Simulation of Arithematic /logic operator circuits using verilog/VHDL
2. Modeling of Combinational/Sequential Circuits Using Verilog HDL
3. Simulation of schematic /RTL using Xilinx ISE Tool
4. ARBITER Design using state diagram in Xilinx ISE Tool
5. Simulation of HDL Netlist using Test bench
6. Modeling of MAC unit using verilog / VHDL
7. Modeling of ALU using verilog / VHDL
8. Design and 8-bit signed multiplication algorithm using verilog / VHDL
9. Design and technological mapping of RTL netlist in Xilinx ISE tool

NOTE: Required Software Tools:

1**.** Mentor Graphic tools / Cadance tools/ Synophysis tools. (180 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 1st Semester –ES		**L**	**T**	**P**	**C**
		2	**0**	**0**	**2**
16ES2111	**TECHNICAL SEMINAR**				

COURSE OUTCOMES:

At the end of the course students able to

1 Analyze and develop a thought process for presentation
2 Improve his language and communication skills
3 Be conversant with the latest developments in power systems

Objectives:

To get involved with the latest advancements and developments to enhance communication and presentation skills, exchange of ideas, greater connectivity to develop a research bent of mind.

For the seminar, the student shall collect the information on a specialized relevant topic and prepare a report, showing his understanding over the topic, and submit the same to the department, which shall be evaluated by the Department Committee consisting of Head of the department, Seminar Supervisor and a Senior Faculty Member. Each Seminar shall be evaluated for 50 marks (10 marks for report, 10 marks for subject content, 20 marks for presentation and 10 marks for queries).

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 2nd Semester –ES

L	T	P	C
3	0	0	3

16ES1201 FPGA ARCHITECTURE AND APPLICATIONS

COURSE OUTCOMES:

At the end of the course students able to

1 Able to gain the knowledge about PLDs, FPGA Design & architectures.
2 Students should be able to understand different types of FSM's
3 Different FSM techniques like ASM and One-hot Design method
4 Understand the various frontend design tools and implementation process.
5 Analyze System level Design and their application for Combinational and Sequential Circuits.

UNIT-I

Programmable Logic: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

FPGA: Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

UNIT-II

Case Studies: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

Finite State Machines(FSM): Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

UNIT-III

Realization of State Machine: Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

FSM Architectures and Systems Level Design: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

UNIT-IV

Digital Front End Digital Design Tools for FPGAS & ASICS: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

TEXT BOOKS:

1 P.K.Chan & S. Mourad, *Digital Design Using Field Programmable Gate Array*, Prentice Hall, 1994.

REFERENCE BOOKS:

1 S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publications, 1994.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 2nd Semester –ES

L	T	P	C
3	0	0	3

16ES1202 REAL TIME OPERATING SYSTEMS

COURSE OUTCOMES:

At the end of the course students able

1 To distinguish a real-time system from other systems.
2 To identify the functions of operating system.
3 To evaluate the need for real-time operating system.
4 To implement the real-time operating system principles.
5 To analyze the case studies like VX works, RT Linux.
6 To understand the fault tolerance techniques in real time operating systems.

UNIT-I

Introduction to UNIX: Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

Real Time Systems: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

UNIT-II

Approaches to Real Time Scheduling: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

Operating Systems: Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

UNIT-III

Fault Tolerance Techniques: Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

Case Studies – VX Works: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

UNIT-IV

RT Linux: Process Management, Scheduling, Interrupt Management, and Synchronization

TEXT BOOKS:

1 Richard Stevens, *Advanced Unix Programming*,
2 Jane W.S. Liu, Real Time Systems, Pearson Education.
3 C.M.Krishna, KANG G. Shin, Real Time Systems, McGraw.Hill

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 2nd Semester –ES

L	T	P	C
3	0	0	3

16ES1203 SYSTEM ON CHIP ARCHITECTURE

COURSE OUTCOMES:

At the end of the course students able to

1 Modeling and simulation of digital VLSI systems using hardware design language
2 To understand SOC architecture and instruction set.
3 Explain how design platforms can be used for an efficient design process
4 To understand soc interconnect architectures and understand bus structures.
5 Describe the design process for complex systems-on-chip
6 To analyze the soc system memory and cache memory.

UNIT-I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT-III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1 Michael J. Flynn and Wayne Luk, Computer System Design System-on-Chip, Wiely India Pvt. Ltd.
2 Steve Furber, ARM System on Chip Architecture,2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1 Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2 Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3 System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 2nd Semester –ES	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

16ES1204 CRYPTOGRAPHY AND NETWORK SECURITY

COURSE OUTCOMES:

At the end of the course students able to

1 To identify common network security vulnerabilities/attacks
2 To explain the foundations of Cryptography and network security
3 To demonstrate detailed knowledge of the role of encryption to protect data.
4 To analyze security issues arising from the use of certain types of technologies.
5 To identify the appropriate procedures required to secure networks.
6 To analyze and design network security protocols.

UNIT-I

Symmetric Ciphers: Overview – classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

Public – Key Encryption and Hash Functions: Introduction to Number Theory, Public-Key Cryptography and RSA, Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

UNIT-II

Network Security Practice: Authentication Applications, Kerbors, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

System Security: Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

UNIT-III

Wireless Security: Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

Secure Networking Threats: Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

UNIT-IV

Encryption Techniques: Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

Designing Secure Networks: Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, the Difficulties of Secure Networking, Security Technologies, Emerging Security Technologies General Design Considerations, Layer 2 Security Considerations, IP Addressing Design Considerations - ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

TEXT BOOKS:

1 William Stallings, Cryptography and Network Security Principles And Practices, 3rd ed., PearsEducation, 2003.
2 Sean Convery, Network Security Architectures, 1st ed., Cisco Press, 2004.

REFERENCE BOOKS:

1 Atul Kahate, Cryptography and Network Security,2nd ed., Tata McGraw Hill, 2003.
2 Bruce Schneier, Applied Cryptography, 2nd ed., John Wiley and Sons Inc, 1996.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 2nd Semester –ES	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

16ES1205 HARDWARE SOFTWARE CO-DESIGN

COURSE OUTCOMES:

At the end of the course students able to

1 Analyze hardware-software co-design problems for systems with moderate complexity.
2 Apply hardware-software co-design methods and techniques to practical problems.
3 Designing hardware-software co-design solutions through SoPC and similar technologies.
4 Applying different levels of abstractions and provide models for verification of the architecture and functionality for embedded co-design solutions.
5 Evaluate and compare quality solutions compared to for example: performance, cost, security, power consumption and size.
6 Partition and design space exploration with LYCOS

UNIT-I

Co-Design Issues: Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware- software partitioning distributed system co-synthesis.

UNIT-II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III

Compilation Techniques and Tools for Embedded Processor:

Architectures: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT-IV

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS:

1 Jorgen Staunstrup, Wayne Wolf, *Hardware / software co- design Principles and Practice*, Springer, 2009.
2 *Hardware / software co- design Principles and Practice*, 2002, Kluwer Academic Publishers

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 2nd Semester –ES	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

16ES1206 **ROBOTIC TECHNOLOGY**

COURSE OUTCOMES:

At the end of the course students able to

1 Study the definition, history ,future trends, classification ,configuration of robot
2 Learn the concepts of matrix algebra, Homogeneous coordinate transformation
3 Analyze the Velocity Kinematics and Iterative Newton –Euler's dynamic formulation
4 Get the knowledge on robot sensors and Trajectory Planning
5 Understand concepts of Micro-robotics and MEMS

UNIT-I

Robot Fundamentals: Definitions, History of robots, present and future trends in robotics, Robot classifications,Robot configurations, Point to Point robots, Continuous Path robots, Work volume, Issues in design and controlling robots Repeatability, Control resolution, spatial resolution, Precision,Accuracy, Robot configurations, Point to Point robots, Continuous Path robots, Work volume, Applications of robots. Drives used in robots-Hydraulic, Pneumatic and Electric drives, Comparison of drive systems and their relative merits and demerits.

UNIT-II

Manipulator Kinematics: Matrix Algebra, Inverse of matrices, rotational groups, matrix representations of coordinate transformation, transformation about reference frame and moving frame Forward & Inverse Kinematics examples of 2R, 3R & 3P manipulators, Specifying position and orientation of rigid bodies Euler's angle and fixed rotation for specifying position and orientation Homogeneous coordinate transformation and examples D-H representation of kinematics linkages Forward kinematics of 6R manipulators using D-H representations Inverse kinematics of 6R manipulators using D-H representations, Inverse Kinematics geometric and algebraic methods.

UNIT-III

Robotics Dynamics: Velocity Kinematics, Acceleration of rigid body, mass distribution Newton's equation,Euler's equation, Iterative Newton –Euler's dynamic formulation, closed dynamic, Lagrangian formulation of manipulator dynamics, dynamic simulation, computational consideration.

Trajectory Planning: Introduction, general considerations in path description and generation, joint space schemes, Cartesian, space schemes, path generation in runtime, planning path using dynamic model point to point and continuous trajectory, 4-3-4 & trapezioidal velocity strategy for robots.

UNIT-IV

Robot Sensors: Internal and external sensors, position- potentiometric, optical sensors ,encoders - absolute, incremental, touch and slip sensors velocity and acceleration sensors, proximity sensors,force & torque sensors, laser range finder, camera. Micro-controllers, DSP, centralized controllers, real time operating systems.

Robot Controllers: Essential components-Drive for Hydraulic and Pneumatic actuators, H-bridge drives for Dc motor, Overload over current and stall detection methods, example of a micro-controller/ microprocessor based robot Controller.

Robot Vision: Introduction, Image acquisition, Illumination Techniques, Image conversion, Cameras, sensors, Camera and system interface, Frame buffers and Grabbers, Image processing, low level & high level machine vision systems.

Futuristic topics in Robotics: Micro-robotics and MEMS (Microelecto mechanical systems), fabrication technology for Micro-robotics, stability issue in legged robots, under-actuated manipulators.

TEXT BOOKS:

1 S.R.Deb, *Robotics Technology and Flexible Automation* , Tata Mc Graw Hill 1994.
2 M.P.Groover, M. Weiss R.N. Nagel, N.G. Odrey, *Industrial Robotics (Technology, Programming and applications)* , McGraw, Hill 1996.
3 K.S.Fu, R.C.Gonzalez and C.S.G.Lee, *Robotics : Control , sensors , vision and intelligence* McGraw- Hill, 1987.
4 J.J.Craig , *Introduction to Robotics* , Addision-wesely 1989

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 2nd Semester –ES	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

16ES1207 **EMBEDDED NETWORKS**

COURSE OUTCOMES:

At the end of the course students able to

1 Learn different type of communication protocols
2 Study the concepts of USB,CAN bus and a simple application
3 Learn the elements ,architecture and working principle of Ethernet
4 Study about the embedded Ethernet
5 Understand the concepts of Wireless Embedded Networking

UNIT-I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT-II

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT-III

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT-IV

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization – Time Synchronization - Energy efficient MAC protocols – SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS:

1 Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2 Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS:

1 Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series – Dogan Ibrahim, Elsevier 2008.
2 Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3 Networking Wireless Sensors - Bhaskar Krishnamachari, Cambridge press 2005.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 2nd Semester –ES	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

16ES1208 **SOFTWARE DEFINES RADIO**

COURSE OUTCOMES:

At the end of the course students able to

1 Understand the concepts of Software radio
2 Learn the Object oriented software radio and its configartion
3 Study of the CORDIC algorithm and filters
4 Analyze the transmitter and receiver architectures
5 Identify the switches ,power amplifiers, technology and modeling
6 Analyze case studies in software radio design.

UNIT-I

Software radio concepts, design principles, receiver front end topologies, noise and distortion in RF chain,digital generation of signals, common ADC and DAC architectures.

UNIT-II

Object oriented software radios, Transmitter configuration, Digital compensation for analog I/O modulator errors, direct digital synthesizers, recursive oscillator.

UNIT-III

CORDIC algorithm, pulse shaping and interpolation filters, resampling, DDS with tunable DSM, digital quad modulator, transmitter and receiver architectures.

UNIT-IV

Power amplifier, switches, components, technology and modeling, case studies in software radio design.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 2nd Semester –ES

L	T	P	C
0	0	3	2

16ES1209 RTOS AND FPGA LAB

COURSE OUTCOMES:

At the end of the course students able to

1 familiarize the RTOS System solution & tools
2 Study the Testing RTOS Environment and System Programming in keil and Tornado tools.
3 Implementation of Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)
4 Implementation of Synthesis of Sequential Circuits

LIST OF EXPERIMENTS

1. RTOS System solution & tools
2. Testing RTOS Environment and System Programming.
   a) Keil Tools
   b) RTOS System Solutions with Tornado tools.
3. Embedded DSP based System Designing.
   a) Code compressor studio (CCS) for embedded DSP using Texas tool kit.
   b) Analog DSP tool kit.
4. Synthesis of the designs made using "VHDL / VERILOG and Mixed Design (VHDL & Verilog)" after Simulation is to be verified using FPGA/CPLD blocks from different commercially available Products on:

a) Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)
b) Synthesis of Sequential Circuits – 6 to 8 MSI and 1 or 2 VLSI Circuits.

NOTE: Required Software Tools for FPGA:

1. Mentor Graphic tools / Cadance tools/ Synophysis tools. (180 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 2nd Semester –ES

L	T	P	C
0	0	3	2

16ES2210 ADVANCED EMBEDDED SYSTEMS LAB

COURSE OUTCOMES:

At the end of the course students able to

1 Familiarize with the ALP and C program using RTOS 8051 kits.
2 Dump the programs into the microcontroller kits using flash magic software.
3 Study ARM evaluation board and familiarize with basic programming concepts.
4 write programs to interface various I/O devices with PIC micro controllers

LIST OF EXPERIMENTS

1. PIC Programming and Interfacing.
   a) Program for addition of BCD numbers.
   b) Interface an LED array and 7-segment display
   c) Interfacing of PIC with LCD
   d) Interfacing of PIC with Keyboard Interfacing
   e) Interfacing of PIC with ADC, DAC
   f) Interfacing of PIC with temperature Sensor
   g) Interfacing of PIC with RTC
   h) Interfacing of PIC with DC Motor Control
   i) Interfacing of PIC with Stepper Motors

2. ARM Programming and Interfacing.
   (a) Introduction to ARM Development Tools.
   (b) Simple ARM Assembly Language and C Programming using ARM Kits.
   (c) LCD Interfacing.
   (d) Timer and Counter Programming.
   (e) Interfacing with Data Converters.
   (f) Serial Port Programming.
   (g) Interfacing with Sensors & Motors.
   (h) Generation of PWM.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 2nd Semester –ES	**L**	**T**	**P**	**C**
	2	**0**	**0**	**2**

16ES2211 **TERM PAPER**

The Term Paper is a precursor to the project work done in the 2nd year M.Tech Programme. The paper may be of 8-10 (A4 size) in length and follows the standard IEEE/Technical Journal Format.

The Term Paper helps to supplement the second year Project Work of the M.Tech students. It helps to identify their Research area/topic and complete the groundwork and preliminary research required for it comfortably. It trains the students to make use of Research Tools and Material available both in print and digital formats.

Based on the topic, a hypothesis is to be made by the student, under the supervision of the guide. The student is then required to collect literature and support information for his / her term paper from Standard Reference Books, Journals, and Magazines - both printed and online. Each student should refer to a minimum of 6 reference sources related to the topic. The student also presents his/her paper with the help of Power Point slides / OHP.

The Term Paper contains: The Aim and Objective of the study, The need for Rationale behind the study, Identify the work already done in the field, Hypothesis and Discussion, Conclusion Appendix with support data (Illustrations, Tables, Graphs, etc.).

Page Limit: minimum of eight pages.

Date of evaluation: During the Lab Internal Exam.

Method of Evaluation: Total 50 marks

1. Day to day work - 10 marks
2. Term Paper Report - 20 marks
3. Seminar - 20 marks

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech 2nd Semester –ES **L T P C**

16ES2212 COMPREHENSIVE VIVA-VOCE

COURSE OUTCOMES:

At the end of the course students able to

1 Test the learning and understanding during the course of under graduate program.
2 Face interview both at the academic and the industrial sector.

All the students shall face a Comprehensive viva-voce covering the total courses of first and second semesters. The comprehensive viva-voce will be conducted along with 2nd semester lab examination for 75 marks by a committee consisting of Head of the Department, two senior faculty members nominated by the Head of the Department

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 3rd Semester –ES	**L**	**T**	**P**	**C**
	0	**0**	**0**	**4**

16ES2301 INTERNSHIP + PROJECT WORK

COURSE OUTCOMES:

At the end of the course students able to

1 develop awareness, understanding and capacity in the specific roles and responsibilities in an industry
2 develop and refinement of technical and professional skills

All the students shall undergo the summer internship during summer break after 2nd semester. The minimum internship period is eight weeks and the students have an option of choosing their own industry/area of interest, which may be related to their respective branch or any other service oriented task. A self study report for the internship shall be submitted and evaluated during the 3rd semester and will be evaluated for a total of 75 marks consisting of 25 marks for internal assessment and 50 marks for semester end examination. Internal assessment shall be done by the internship supervisor. Semester end examination for 50 marks shall be conducted by two examiners, one of them being internship supervisor as internal examiner and an external examiner nominated by the Principal from the panel of experts recommended by HOD

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

M.Tech 4th Semester –ES	**L**	**T**	**P**	**C**
	0	0	0	20

16ES2401 **PROJECT WORK**

COURSE OUTCOMES:

At the end of the course students able to

1 Identify a problem of current relevance to society
2 Formulate the problem and identify suitable modeling paradigm.
3 Analyze the problem and identify the solution methodology

Students are required to take up a project work, in which the student can choose any specific problem of Industry or Industry based project work. Alternatively it can be secondary source based or Field based project work. Before the commencement of the project work each student is required to submit a synopsis indicating the objectives, Methodology, Framework for analysis, Action plan with milestones in order to have clarity for the subsequent work. The project should have an internal faculty as guide. The student can initiate the project work in the penultimate semester of the course.