AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
Gudur, Nellore Dist - 524101, A.P (India)

ACADEMIC REGULATIONS FOR THE AWARD OF FULL TIME
M.Tech DEGREE PROGRAMME
(WITH EFFECT FROM THE ACADEMIC YEAR 2013-14)

The **Audisankara College of Engineering and Technology**, Gudur, Nellore District, Andhra Pradesh shall confer M.Tech Post Graduate degree to candidates who are admitted to the Master of Technology Programs and fulfill all the requirements for the award of the degree.

1. ELIGIBILITY FOR ADMISSIONS:

Admission to the Master of Technology programme shall be made subject to the eligibility, qualifications and specialization criteria prescribed by the JNTUA, Anantapur for each programme, from time to time.

As per the norms of A.P. State Council of Higher Education (APSCHE), Government of Andhra Pradesh, admissions are made to the first year of two years M.Tech P.G. Degree Programme as follows:-

- As per the norms of Government of Andhra Pradesh, Category-A (based on the rank obtained in GATE / PGECET score) seats will be filled by the Convener, PGECET.
- As per the norms of Government of Andhra Pradesh, Category-B seats will be filled by the management.

2. COURSE WORK:

- A Candidate after securing admission must pursue the M.Tech course of study for Four Semesters duration.
- Each semester shall be of 20 weeks duration including all examinations.
- A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

3.0 ATTENDANCE REGULATIONS AND CONDONATION:-

(i) A student shall be eligible to appear for end semester examinations, if he acquires a minimum of 75% attendance in aggregate of all the subjects.

(ii) Condonation of shortage of attendance in aggregate up to 10% on medical grounds (65% above and below 75%) in each semester may be granted on the recommendation of the College Academic Committee. However, granting condonation is purely at the discretion of Principal of the college.

(iii) A Student will not be promoted to the next semester unless he satisfies the attendance requirement of the present semester as applicable. They may seek re-admission for that semester as and when offered next.

(iv) Shortage of Attendance below 65% in aggregate shall in no case be condoned.

(v) Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examinations of that particular semester and their registration for examination shall stand cancelled.

(vi) A stipulated fee shall be payable towards condonation of shortage of attendance if granted.

(vii) Attendance may also be condoned for those students who participate in prestigious sports and co and extracurricular activities provided their attendance is in the minimum prescribed range for the purpose and recommended by the concerned authority.

4.0. EVALUATION:-

The performance of the candidate in each semester shall be evaluated subject-wise for a maximum of 100 marks for Theory and 100 marks for practical subjects, on the basis of Internal Evaluation and End Semester Examination. For the theory & practical subjects 60% of the marks will be for the External End Examination, while 40% of the marks for Internal Evaluation.

4.1 INTERNAL EVALUATION FOR THEORY SUBJECTS:

Each course is evaluated for **40** marks **(a+b)**

a) Two Midterm Examinations each for **30 marks** with a duration of two hours each will be conducted for every theory course in a semester. First Midterm Examination is conducted in the middle of the Semester (I & II units) and second Midterm Examination immediately after the completion of instruction (III & IV units) as per academic schedule. The Midterm Examination marks shall be awarded giving a weightage of 80% in the Midterm Examination in which the student scores more marks and 20% in the remaining Midterm Examination.

Midterm Examination Pattern for 30 Marks:

- Each Midterm Examination Question Paper comprises of four questions covering the two units.
- Answering any three questions.
- Questions 1 & 2 from one unit and Questions 3 & 4 from another unit. Each question is allotted 10 marks.

b) 10 marks are allocated for **Assignment Tests.**

- There will be four Assignment Tests per subject.
- One Assignment Test is conducted from each unit.
- Five Assignment questions are given in advance from each unit out of which two questions given by the concerned teacher has to be answered during Assignment Test.
- Average of Assignment Tests marks is considered.

NOTE: A student who is absent for any Midterm Examination / Assignment Test, for any reason whatsoever, shall be deemed to have scored zero marks in that Midterm Examination/ Assignment Test and no make-up test shall be conducted.

4.2 INTERNAL EVALUATION FOR PRACTICAL SUBJECTS:

For Laboratory courses there shall be continuous evaluation during the semester for 40 internal marks. The break-up of internal marks to be awarded is as given below:

Table 1: Break-up of Internal Marks

S.No.	Criterion	Marks
1	Conduct of experiments, Observation & Results in regular class work(Day-to-Day Performance)	25
2	Viva – voce and Internal Examination	15

In any semester a minimum of 90% of the prescribed number of experiments/exercises specified in the syllabus for laboratory course shall be conducted. They shall complete these experiments/exercises in all respects and submit report and get it certified by the concerned internal lab teacher and the Head of the Department to become eligible to appear for the final end examination in the Laboratory Course.

4.3 INTERNAL EVALUATION FOR SEMINAR-I & SEMINAR-II:

There shall be two Seminars conducted in each discipline, Seminar-I in the M.Tech I Semester and the Seminar-II in M.Tech IV semester. The distribution of internal marks for seminar is given below:

Table 2: Distribution of Marks

S.No.	Criterion	Marks
1	Seminar Report & Subject content	20
2	Seminar presentation & Viva – Voce Exam	30

For the seminar, the student shall collect the information on a specialized relevant topic and prepare a report, showing his understanding over the topic, and submit the same to the department, which shall be evaluated by the Department Committee consisting of Head of the department, Seminar Supervisor and a Senior Faculty Member. Each Seminar shall be evaluated for 50 marks (10 marks for report, 10 marks for subject content, 20 marks for presentation and 10 marks for queries).

4.4 TERM PAPER:

The Term Paper is a precursor to the project work done in the 2nd year M.Tech Programme. The paper may be of 8-10 (A4 size) in length and follows the standard IEEE/Technical Journal Format.

The Term Paper helps to supplement the second year Project Work of the M.Techstudents. It helps to identify their Reserch area/topic and complete the groundwork andpreliminary research required for it comfortably. It trains the students to make use of Research Tools and Material available both in print and digital formats.
Based on the topic, a hypothesis is to be made by the student, under the supervision of the guide. The student is then required to collect literature and support information for his / her term paper from Standard Reference Books, Journals, and Magazines - both printed and online. Each student should refer to a minimum of 6 reference sources related to the topic. The student also presents his/her paper with the help of Power Point slides / OHP.
The Term Paper contains: The Aim and Objective of the study, The need for Rationale behind the study, Identify the work already done in the field, Hypothesis and Discussion, Conclusion Appendix with support data (Illustrations, Tables, Graphs, etc.).
Page Limit: minimum of eight pages.
Date of evaluation: During the Lab Internal Exam.
Method of Evaluation**:** Total 50 marks
1. Day to day work - 10 marks
2. Term Paper Report - 20 marks
3. Seminar - 20 marks

4.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

4.6 In case the candidate does not secure the minimum academic requirement in any subject(as specified in 4.4) he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the course when next offered or do any other specified subject as may be required.

5.0 SEMESTER END EXAMINATIONS:-

5.1 Theory Courses: 60 marks each

The Semester end examination in each theory subject shall be conducted for 3 hours duration at the end of the semester for 60 marks. The question paper for Semester pattern shall be designed as per the following:

Question paper contains

- A total of Eight questions.
- Answer one Question from each Unit
- The Eight questions are to be designed taking one question from each unit (Unit Wise Either or Type) of the four units.
- In each question, one, two or more bits can be set, totaling 15 Marks with appropriate distribution of marks.

A student has to secure not less than a minimum of 40% of marks (24 marks) exclusively at the end semester examinations in each of the theory subjects in which the candidate had appeared. However, the candidate shall have to secure a minimum of 50% of marks (50 marks) in both external and internal components put together to become eligible for passing in the subject.

5.2 Lab Courses (Practical / Workshop): 60 marks

Out of 60 marks **40** marks are allocated for experiment (procedure for conducting the experiment carries 10 marks & readings, calculation and result-30 marks) and **15** marks for viva-voce examination with **5** marks for the record.

Each Semester External Lab Examination shall be evaluated by an Internal Examiner along with an External Examiner. External Examiner is appointed by the Principal.
A candidate shall be declared to have passed in individual lab course if he secures a minimum of 50% aggregate marks (50 marks) (Internal & Semester External Examination marks put together), subject to a minimum of 40% marks (24 marks) in the semester external examination.

5.3 EVALUATION OF PROJECT WORK:-

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ concerned department.

- **Registration of Project work**: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Semesters)
- An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor/ Guide and one Internal senior expert shall monitor the progress of the project work.
- The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest and one calendar year from the date of registration for the project work. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

- The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.
- A candidate shall be allowed to submit the thesis / dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva-voce examination of the project. The viva-voce examination may be conducted once in two months for all the candidates submitted during that period.
- Three copies of the Thesis / Dissertation certified in the prescribed form by the supervisor and HOD shall be submitted to the HOD.
- The semester end examination for project work done during III & IV Semesters, shall be conducted by a Project Review Committee (PRC). The evaluation of project work shall be conducted at the end of the IV Semester.
- The PRC comprises of an External examiner appointed by the Principal, Head of the Department and Project Guide/Supervisor to adjudicate the thesis / dissertation. The PRC shall jointly evaluate candidates work and award grades as given below

S.No	Description	Grade
1	Very Good	Grade A
2	Good	Grade B
3	Satisfactory	Grade C
4	Not satisfactory	Grade D

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the thesis.

6.0 RE-REGISTRATION FOR IMPROVEMENT OF INTERNAL EVALUATION MARKS:

Following are the conditions to avail the benefit of improvement of internal evaluation marks.

- The candidate should have completed the course work and obtained examinations results for I & II semesters.
- He should have passed all the subjects for which the internal evaluation marks secured are more than 50%.
- Out of the subjects the candidate has failed in the examination due to Internal evaluation marks secured being less than 50%, the candidate shall be given one more chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.
- The candidate has to re-register for the subjects so chosen and fulfill all the academic requirements.
- For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of **'The Principal, Audisankara College of Engineering & Technology' payable at Gudur** along with the requisition through the Controller of the Examinations of the college.
- In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

7.0 SEMESTER – WISE DISTRIBUTION OF CREDITS:

Table 3: Semester –wise Credits distribution

SEMESTER	No. of Credits per semester Theory + Lab	Total credits
I Semester	24+06	30
II Semester	24+06	30
III & IV Semesters	0+18	18
TOTAL CREDITS	48+30	78

8.0 AWARD OF DEGREE AND CLASS:-

A candidate shall be eligible for the award of degree if he satisfies the minimum academic requirements in every subject, Seminar and secures 'satisfactory' or higher grade report on his thesis/dissertation and viva-voce. Based on overall percentage of marks obtained, the following class is awarded.

Table 4: Award of Division

Class Awarded	% of marks to be secured
First Class with Distinction	70% and above
First Class	Below 70% but not less than 60%
Second Class	Below 60% but not less than 50%

9.0 READMISSION CRITERIA:

A Candidate, who is detained in a semester due to lack of attendance, has to obtain written permission from the Principal for readmission into the same semester after duly fulfilling all the required norms stipulated by the college in addition to paying the required fee.

10. SUPPLEMENTARY EXAMINATIONS:

Apart from the regular End Examinations the institute may also schedule and conduct supplementary examinations for all subjects for the benefit of students with backlogs. Such students writing supplementary examinations as supplementary candidates may have to write more than one examination per day.

11.CONDUCT AND DISCIPLINE:-

(a) Students shall conduct themselves within and outside the premises of the Institute in a descent and dignified manner befitting the students of ACET.

(b) As per the order of the Honorable Supreme Court of India, ragging in any form is considered a criminal offence and is totally banned. Any form of ragging will be severely dealt with.

(c) The following acts of omission and / or commission shall constitute gross violation of the code of conduct and are liable to invoke disciplinary measures with regard to ragging.
   (i) Lack of courtesy and decorum; indecent behavior anywhere within or outside the college campus.
   (ii) Damage of college property or distribution of alcoholic drinks or any kind of narcotics to fellow students / citizens.

(d) Possession, consumption or distribution of alcoholic drinks or any kind of narcotics or hallucinogenic drugs.

(e) Mutilation or unauthorized possession of library books.

(f) Noisy and unruly behavior, disturbing studies of fellow students.
(g) Hacking in computer systems (such as entering into other person's areas without prior permission, manipulation and / or damage of computer hardware and software or any other cyber crime etc.
(h) Usage of camera /cell phones in the campus.
(i) Plagiarism of any nature.
(j) Any other act of gross indiscipline as decided by the college academic council from time to time.
(k) Commensurate with the gravity of offense, the punishment may be reprimand, fine, expulsion from the institute/ hostel, debarring from examination, disallowing the use of certain facilities of the Institute, rustication for a specified period or even outright expulsion from the Institute, or even handing over the case to appropriate law enforcement authorities or the judiciary, as required by the circumstances.
(l) For an offence committed in (i) a hostel (ii) a department or in a class room and (iii) elsewhere, the chief Warden, the concern Head of the Department and the Principal respectively, shall have the authority to reprimand or impose fine.
(m) Cases of adoption of unfair means and/ or any malpractice in an examination shall be reported to the principal for taking appropriate corrective action.
(n) All cases of serious offence, possibly requiring punishment other than reprimand, shall be reported to the Academic council of the college.
(o) The Institute Level Standing Disciplinary Action Committee constituted by the academic council shall be the authority to investigate the details of the offence, and recommend disciplinary action based on the nature and extent of the offence committed.
(p) The Principal shall deal with any problem, which is not covered under these rules and regulations.
(q) **"Grievance and Redressal Committee" (General)** constituted by the Principal shall deal with all grievances pertaining to the academic / administrative / disciplinary matters.
(r) All the students must abide by the code and conduct rules prescribed by the college from time to time.

12.0 WITH – HOLDING OF RESULTS:

If the candidate has not paid dues to the university/college or if any case of in-discipline is pending against him, the result of the candidate shall be withheld and he will not be allowed / promoted to the next higher semester. The issuing of degree is liable to be withheld in such cases.

13.0 TRANSITORY REGULATIONS:

Candidates who have discontinued or have been detained for want of attendance or who have failed after having undergone the course in earlier regulations and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when such subjects are offered, subject to the conditions of 4.5 and 2.3 sections.

14.0MINIMUM INSTRUCTION DAYS:

The minimum instruction days for each semester shall be 90 clear instruction days excluding the days allotted for tests/examinations and preparation holidays declared if any.

15.0AMENDMENTS OF REGULATIONS-

The college may, from time to time, revise, amend or change the regulations, scheme of examinations and syllabi. However the academic regulations of any student will be same throughout the course of study in which the student has been admitted.

16.0 GENERAL:

- The academic regulations should be read as a whole for the purpose of any interpretation.
- Disciplinary action for Malpractice/improper conduct in examinations is appended.
- Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.
- In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Head of the Institute is final.

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RULES FOR DISCIPLINARY ACTION FOR MALPRACTICE / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	**Punishment**
	If the candidate	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Is found copying in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate will be cancelled.
3.	Comes in alcohol drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
4.	Smuggles the Answer book or a part there of additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of

		seat.
5.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
6.	Possesses any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate will also be debarred and forfeit the seat.
7.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate will also be debarred and forfeit the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate will also be debarred for two consecutive semesters from class work and all end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case registered against him.
8.	Refuses to obey the orders of the Chief Superintendent/Asst.Superintendent/ any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall causing any injury to him or to any of his relations	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are

	whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case registered against them.
9.	Is a student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clauses 6 to 8.	In case of students of the college expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
11.	Is detected copying on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	Indulging in any malpractice which is not covered in the above clauses 1 to 11 if detected shall be reported to the College Authorities for further action to award suitable punishment.	Appropriate action will be taken as recommended by the College Authorities.

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.

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Course Structure for M.Tech (VLSI) Regular Programme
Applicable for students admitted from Academic Year 2013-14

M.Tech I Year (I Semester) – VLSI

Sl.No	Course Code	Subject	Scheme of instruction (Periods / week)		Scheme of Examination			No. of Credits
			Theory	Lab	IM	EM	Total Marks	
1	13VL101	VLSI Technology	4	-	40	60	100	4
2	13VL102	Analog IC Design	4	-	40	60	100	4
3	13VL103	Digital IC Design	4	-	40	60	100	4
4	13VL104	Hardware Description Languages	4	-	40	60	100	4
5	13VL105	Device Modeling	4	-	40	60	100	4
6	13VL106 13VL107 13VL108	**Elective-I** 1. Embedded System Concepts 2. Scripting Language for VLSI Design Automation 3. ASIC Design	4	-	40	60	100	4
7	13VL109	Analog IC Design Lab	-	3	40	60	100	2
8	13VL110	Digital IC Design Lab	-	3	40	60	100	2
9	13VL111	Seminar-I	-	-	50	-	50	2
Contact Periods / Week			**24**	**6**	**370**	**480**	**850**	
			Total Periods/ Week		**30**	**Total Credits**		**30**

M.Tech I Year (II Semester) – VLSI

Sl.No	Course Code	Subject	Scheme of instruction (Periods / week)		Scheme of Examination			No. of Credits
			Theory	Lab	IM	EM	Total Marks	
1	13VL201	FPGA Architectures and Applications	4	-	40	60	100	4
2	13VL202	Testing & Testability	4	-	40	60	100	4
3	13VL203	Low Power VLSI Design	4	-	40	60	100	4
4	13VL204	Algorithms for VLSI Design Automation	4	-	40	60	100	4
5	13VL205	Hardware Software Co-Design	4	-	40	60	100	4
6	13VL206 13VL207 13VL208	**Elective-II** 1. DSP Processors and Architectures 2. Cryptography and Network Security 3. Real Time Operating Systems	4		40	60	100	4
7	13VL209	Mixed Signal Lab	-	3	40	60	100	2
8	13VL210	Embedded Processing Lab	-	3	40	60	100	2
9	13VL211	Term Paper	-	-	50	-	-	2
Contact Periods / Week			**24**	**3**	**370**	**480**	**850**	
			Total Periods/ Week		**27**	**Total Credits**		**30**

M.Tech II Year (III & IV Semesters) – VLSI

Sl.No	Course Code	Subject	Scheme of Examination			No. of Credits
			IM	EM	Total Marks	
1	13VL401	Seminar-II	50	-	50	2
2	13VL402	Project Work	-	A/B/C/D		16
Contact Periods / Week						**18**
					Total Credits	

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
(AUTONOMOUS)

Detailed Syllabus

M.Tech I Semester (VLSI)	L	T	P	[C]
	4	0	0	[4]

(13VL101) VLSI TECHNOLOGY

UNIT- I:

Review of Microelectronics and Introduction to MOS Technologies: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

Basic Electrical Properties of MOS, CMOS & BICOMS Circuits: Ids -Vds Relationships, Threshold Voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, Zpu/Zpd, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT- II:

Layout Design and Tools: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT- III:

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

Sequential Systems: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT- IV:

Floor Planning & Architecture Design: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

Introduction to CAD Systems (Algorithms) and Chip Design: Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

Text Books:

1. K. Eshraghian et . al(3 authors), Essentials of VLSI Circuits and Systems, , PHI of India Ltd.,2005
2. Wayne Wolf, Modern VLSI Design, 3rd ed., Pearson Education,2005.

Reference Books:

1. N.H.E Weste, K.Eshraghian, Adison Wesley, Principals of CMOS Design, 2nd ed.,1993.
2. Fabricius, Introduction to VLSI Design, MGH International Edition, 1990.
3. Baker, Li Boyce, CMOS Circuit Design, Layout and Simulation, PHI, 2004.

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M.Tech I Semester (VLSI)

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4	0	0	[4]

(13VL102) ANALOG IC DESIGN

UNIT- I:

MOS transistors- Modeling in linear, saturation and cutoff high frequency equivalent circuit.

Integrated Devices and Modeling and Current Mirror: Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load. Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors and Bipolar Gain Stages. Frequency Response.

UNIT- II:

Operational Amplifier Design and Compensation: Two Stage CMOS Operational Amplifier. Feedback and Operational Amplifier Compensation. Advanced Current Mirror. Folded–Cascade Operational Amplifier, Current Mirror Operational Amplifier Fully Differential Operational Amplifier. Common Mode Feedback Circuits. Current Feedback Operational Amplifier. Comparator. Charge Injection Error. Latched Comparator and Bi-CMOS Comparators.

Sample and Hold Switched Capacitor Circuits-I: MOS, CMOS, Bi-CMOS Sample and Hold Circuits. Switched Capacitor Circuits: Basic Operation and Analysis. First Order and Biquard Filters.

UNIT- III:

Sample and Hold Switched Capacitor Circuits-II: Charge Injection. Switched Capacitor Gain Circuit. Correlated. Double Sampling Techniques. Other Switched Capacitor Circuits.

Data Converters: Ideal D/A & A/D Converters. Quantization Noise. Performance Limitations. Nyquist Rate D/A Converters: Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating ,Successive Approximation, Cyclic Flash Type, Two Step, Interpolating, Folding and Pipelined, A/D Converters.

UNIT- IV:

Over Sampling Converters and Filters: Over Sampling With and Without Noise Shaping. Digital Decimation Filter. High Order Modulators. Band Pass Over Sampling Converter. Practical Considerations. Continuous Time Filters.

Text Books:

1. D.A.John, Ken Martin, Analog Integrated Circuit Design", 1st ed., John Wiley, 1996.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuit, Tata-Mc GrawHill, 1st ed.,2002.

Reference Books:

1. Philip Allen & Douglas Holberg, CMOS Analog Circuit Design, Oxford University Press, 3rd ed.,2011.
2. GREGOLIAN &TEMES: Analog MOS Integrated Circuits, John Wiley, 1986.

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(13VL103) DIGITAL IC DESIGN

UNIT- I:

CMOS inverters -static and dynamic characteristics.

Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

UNIT- II:

Method of Logical Effort for Transistor Sizing -power consumption in CMOS gates- Low power CMOS design.

Arithmetic Circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

UNIT- III:

Bipolar gate Design- BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.

Layout Design Rules: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT- IV:

Subsystem Design Process: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

Text Books:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, 2nd ed., MGH,1999.
2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, 2nd ed.,Prentice Hall, 2003.
3. Eugene D Fabricus, Introduction to VLSI Design, McGraw Hill International Edition, 1990.

REFERENCES:

1. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000.
2. Neil H E West and Kamran Eshranghian, Principles of CMOS VLSI Design: A System Perspective",2nd ed., Addision-Wesley,2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation,IEEE Press, 1998.
4. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, 3rd ed., McGraw-Hill, 2004.

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(13VL104) HARDWARE DESCRIPTION LANGUAGES

UNIT- I:

Hardware Modeling with the Verilog HDL: Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

Logic System, Data Types and Operators for Modeling in Verilog HDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT- II:

Behavioral Descriptions in Verilog HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

Synthesis of Combinational Logic: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares, Synthesis of Sequential Logic Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT- III:

Synthesis of Language Constructs: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

Switch – Level Models in Verilog: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

UNIT- IV:

Introduction to HDL: An Overview of Design Procedures used for System Design using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. Design Verification Tools. Examples using Commercial PC Based on VHDL Elements of VHDL Top Down Design with VHDL Subprograms. Controller Description VHDL Operators.

Behavioral Description of Hardware in HDL: Process Statement Assertion Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design. Differences between VHDL and Verilog.

Text Books:

1. M.D.CILETTI, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice-Hall, 1999.
2. Z.NAWABI, VHDL Analysis and Modeling of Digital Systems, 2nd ed., McGraw Hill, 1998.

Reference Books:

1. M.G.ARNOLD, Verilog Digital – Computer Design, Prentice-Hall (PTR), 1999.
2. PERRY, VHDL, 3rd ed., McGraw Hill.

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(13VL105) DEVICE MODELLING

UNIT- I:

Basic Semiconductor Physics: Quantum Mechanical Concepts - Carrier Concentration - Transport Equation - Bandgap –Mobility and Resistivity - Carrier Generation and Recombination - Avalanche Process - Noise Sources.

UNIT- II:

Bipolar Device Modeling: Injection and Transport Model - Continuity Equation - Diode Small Signal and Large Signal (Change Control Model) - Transistor Models: Ebber - Molls and Gummel Port Model – Mextram model - SPICE modeling temperature and area effects.

UNIT- III:

MOSFET Modeling: Introduction - Inversion Layer - MOS Transistor Current - Threshold Voltage - Temperature Short Channel and Narrow Width Effect - Models for Enhancement - Depletion Type MOSFET -CMOS Models in SPICE.

UNIT- IV:

Parameter Measurement: General Methods - Specific Bipolar Measurement - Depletion Capacitance - Series Resistances -
Early Effect - Gummel Plots - MOSFET: Long and Short Channel Parameters - Statistical Modeling of Bipolar and MOS Transistors.

Optoelectronic Device Modeling: Static and Dynamic Models - Rate Equations - Numerical Technique - Equivalent Circuits -Modeling of LEDs - Laser Diode and Photo detectors.

Text Books:

1.Philip E. Allen, Douglas R.Hoberg, CMOS Analog Circuit Design, 2nd ed., Oxford Press - 2002.
2. Kiat Seng Yeo, Samir S.Rofail, Wang-Ling Gob, CMOS / BiCMOS ULSI - Low Voltage, Low Power, Person Education, 2003.

Reference Books:

1. Sze S.M. “Semiconductor Devices - Physics and Technology”, John Wiley and sons, 1985.
2. Giuseppe Massobrio and Paolo Antogentti, Semiconductor Device Modeling with SPICE,2nd ed.,, McGraw-Hill Inc, New York, 1993.
3. Mohammed Ismail & Terri Fiez “Analog VLSI-Signal & Information Processing, 1st ed., Tata McGraw Hill Publishing company Ltd, 2001.

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(13VL106) EMBEDDED SYSTEM CONCEPTS
(ELECTIVE-I)

UNIT- I:

Introduction to Embedded Systems: An Embedded System, Processor in The System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System -On-Chip (SOC) and in VLSI Circuit.

Processor and Memory Organization: Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

UNIT- II:

Devices and Buses for Device Networks: I/O Devices, Timer and Counting Devices, Serial Communication Using The "I^2C" , CAN, Profibus Foundation Field Bus. and Advanced I/O Buses Between the Network Multiple Devices, Host Systems or Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses.

Device Drivers and Interrupts Servicing Mechanism: Device Drivers, Parallel Port and Serial Port Device Drivers in a System, Device Drivers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

UNIT- III:

Instruction Sets: Introduction, preliminaries, ARM processor, SHARC processor.

Programming Concepts and Embedded Programming in C, C++, VC++ and JAVA: Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

UNIT- IV:

Hardware- Software C0- Design in an Embedded System: Embedded System Project Management, Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, use of Target Systems, use of Software Tools for Development of an Embedded System, use of Scopes and Logic Analysis for System, Hardware Tests. Issues in Embedded System Design.

Text Books:

1. Rajkamal, Embedded systems: Architecture, Programming and Design, TMH, 2008.
2. wayne wolf, Computers as a component: principles of embedded computing system design.

Reference Books:

1. Arnold S Berger, Embedded System Design, 1st ed., CMP Books, 2001.
2. An embedded software primer by David Simon, 1st Indian Reprint, PEA, 2001.
3. Steve Heath, Embedded systems design: Real world design , Newton Mass USA, 2002.
4. Hayt, Data communication.

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(13VL107) SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION (ELECTIVE-I)

UNIT- I:
Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.

UNIT- II:
Inter process Communication Threads, Compilation & Line Interfacing.

UNIT- III:
Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL .

UNIT- IV:
Other Languages: Broad Details of CGI, VB Script, Java Script with Programming Examples.

Text Books:
1.Randal L, Schwartz Tom Phoenix, Learning PERL, 3rd ed., Oreilly Publications, 2000
2.Larry Wall, Tom Christiansen, John Orwant, Programming PERL, 3rd ed., Oreilly Publications 2000.
3.Tom Christiansen, Nathan Torkington, PERL Cookbook, 3rd ed., Oreilly Publications, 2000.

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(13VL108) ASIC DESIGN
(ELECTIVE-I)

UNIT- I:

ASIC Design Styles: Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs.

ASICS – Programmable Logic Devices: Overview – PAL –based PLDs: Structures; PAL Characteristics – FPGAs: Introduction, selected families – design outline.

UNIT II

ASICS –Design Issues: Design methodologies and design tools – design for testability – economies.

ACISS Characteristics and Performance: design styles, gate arrays, standard cell -based ASICs, Mixed mode and analogue ASICs.

UNIT- III:

ASICS-Design Techniques: Overview- Design flow and methodology-Hardware description languages-simulation and checking-commercial design tools- FPGA Design tools: XILINX, ALTERA

Logic Synthesis, Simulation and Testing: Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation- automatic test pattern generation.

UNIT- IV:

ASIC Construction: Floor planning, placement and routing system partition.

FPGA Partitioning: Partitioning Methods-Floor Planning- Placement-Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

Text Books:

1. L.J.Herbst, Integrated Circuit Engineering, OXFORD SCIENCE Publications, 1996.

Reference Books:

1. M.J.S.Smith, Application - Specific integrated circuits, Addison-Wesley Longman Inc ,1997.

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(13VL109) ANALOG IC DESIGN LAB

1. **NMOS Inverter:**

Depletion and Enhancement Mode Circuit Simulation and Adjustment of Vh VLSI Vm parameters for NMOS inverter.

2. **CMOS Inverter:**

Circuit Simulation, adjustment of W / L ratio of P & N channel MOS transistor for symmetrical drive output and loading consideration. Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners).

Layout of CMOS Inverter, Extraction of parasitic and back annotation and related modifications in circuit parameters and layout.

3. **Current Source / Mirror:**

Circuit simulation of current Mirror using BJT and MOS (Simple, Wilson and Widler configurations) study and modifications to improve power and load regulation. Layout of CMOS Current Mirror.

4. **8 Bit shift register cell:**

Building of cell Library of logic gates and flip flops and building of 8 bit shift register from the same. Optimization of the same from layout and power considerations.

5. **Differential Amplifier:**

Study of specifications of Differential amplifier and Design considerations. Study of input loading and biasing techniques.

Tools required: Mentor Graphic tools / Cadance tools/ Synophysis tools/Microwind. (180 nm Technology and Above)

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(13VL110) DIGITAL IC DESIGN LAB

1. Digital Circuits Description using Verilog and VHDL.
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits.
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

NOTE: Required Software Tools:

1**.** Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)

2. Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

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(13VL111) SEMINAR-I

Objectives: To get involved with the latest advancements and developments to enhance communication and presentation skills, exchange of ideas, greater connectivity to develop a research bent of mind.

For the seminar, the student shall collect the information on a specialized relevant topic and prepare a report, showing his understanding over the topic, and submit the same to the department, which shall be evaluated by the Department Committee consisting of Head of the department, Seminar Supervisor and a Senior Faculty Member. Each Seminar shall be evaluated for 50 marks (10 marks for report, 10 marks for subject content, 20 marks for presentation and 10 marks for queries).

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(13VL201) FPGA ARCHITECTURES AND APPLICATIONS

UNIT- I:

Programmable Logic: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

FPGA: Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

UNIT- II:

Case Studies: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

Finite State Machines(FSM): Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

UNIT- III:

Realization of State Machine: Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

FSM Architectures and Systems Level Design: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

UNIT- IV:

Digital Front End Digital Design Tools for FPGAS & ASICS: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

Text Books:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall, 1994.
2. S.Trimberger , Field Programmable Gate Array Technology, Kluwer Academic Publications,1994.

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(13VL202) TESTING AND TESTABILITY

UNIT- I:

Introduction to Test and Design for Testability (DFT) Fundamentals: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

Fault Modeling: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

UNIT- II:

Testing for Single Stuck Faults (SSF): Automated Test Pattern Generation (ATPG/ATG) For Ssfs In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models. Vector Simulation – ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

Design for Testability: Testability Trade-Offs, Techniques. Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design. Board Level and System Level DFT Approaches. Boundary Scans Standards. Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT- III:

Built – in Self – Test (BIST): BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT- IV:

Memory BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

Brief Ideas on Embedded Core Testing: Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

Text Books:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, 1st ed., Jaico Publishing House, 2001.

Reference Books::

1. Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall, 1999.
2. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, 1998.

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(13VL203) LOW POWER VLSI DESIGN

UNIT- I:

Low Power Design, an Over View: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS Processes: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT- II:

Low-Voltage/Low Power CMOS/ BICMOS Processes: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT- III:

CMOS and Bi-CMOS Logic Gates: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

Low- Voltage Low Power Logic Circuits: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT- IV:

Low Power Latches and Filip Flops: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

Special Techniques: Power Reduction in Clock Networks, CMOS Floating Node,Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

Text Books:

1. Yeo Rofail/ Gohl(3 Authors), "CMOS/BiCMOS ULSI low voltage, low power", Pearson Education Asia, 1st Indian reprint,2002.
2. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP, 2002.

Reference Books:

1. Douglas A.Pucknell & Kamran Eshraghian, Basic VLSI Design, 3rd ed., PHI, 2005.
2. J.Rabaey, Digital Integrated circuits, PHI,1996
3. Sung-mo Kang and Yusuf Leblebici, CMOS Digital ICs, 3rd ed., TMH 2003.
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

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(13VL204) ALGORITHMS FOR VLSI DESIGN AUTOMATION

UNIT- I:

Preliminaries: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

General Purpose Methods for Combinational Optimization: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT- II:

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

Modelling and Simulation: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT- III:

Logic Synthesis and Verification: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

High – Level Synthesis: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT- IV:

Physical Design Automation of FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

Physical Design Automation of MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin, Distribution and routing, Routing and Programmable MCM's.

Text Books:

1. S.H.Gerez, Algorithms for VLSI Design Automation, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. Naveed Sherwani, Algorithms for VLSI Physical Design Automation ,3rd ed., Springer International edition, 2005.

Reference Books:

1. Hill & Peterson, Computer Aided Logical Design with Emphasis on VLSI, Wiley, 1993.
2. Wayne Wolf, Modern VLSI Design Systems on silicon, 2nd ed., Pearson Education Asia, 1998.

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(13VL205) HARDWARE SOFTWARE CO-DESIGN

UNIT- I:

Co-Design Issues: Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware- software partitioning distributed system co-synthesis.

UNIT- II:

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT- III:

Compilation Techniques and Tools for Embedded Processor:

Architectures: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT- IV:

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

Text Books:

1. Jorgen Staunstrup, Wayne Wolf, Hardware / software co- design Principles and Practice, Springer,2009.
2. Hardware / software co- design Principles and Practice, Kluwer Academic Publishers , 2002.

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(13VL206) DSP PROCESSORS AND ARCHITECTURES
(ELECTIVE-II)

UNIT- I:

Introduction to Digital Signal Processing Introduction, Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

Computational Accuracy in DSP Implementations

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT- II:

Architectures for Programmable DSP Devices

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Execution Control and Pipelining

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT- III:

Programmable Digital Signal Processors

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

Implementations of Basic DSP Algorithms

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters,Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT- IV:

Implementation of FFT Algorithms

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

Interfacing Memory and I/O Peripherals to Programmable DSP Devices

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

Text Books:

1. Avtar Singh and S. Srinivasan, Digital Signal Processing, Thomson Publications, 2004.
2. Lapsleyetal, DSP Processor Fundamentals, Architectures & Features, S.Chand & Co, 2000.

Reference Books:

1. B. Venkata Ramani, M. Bhaskar, Digital Signal Processors, Architecture, Programming and Applications, 4th ed. Reprint,TMH,2008.
2. Jonatha Stein, Digital Signal Processing ,1st ed., John Wiley, 2005.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR
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M.Tech II Semester (VLSI)

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(13VL207) CRYPTOGRAPHY AND NETWORK SECURITY
(ELECTIVE-II)

UNIT- I:

Symmetric Ciphers: Overview – classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

Public – Key Encryption and Hash Functions: Introduction to Number Theory, Public-Key Cryptography and RSA, Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

UNIT- II:

Network Security Practice: Authentication Applications, Kerbors, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

System Security: Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

UNIT- III:

Wireless Security: Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

Secure Networking Threats: Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

UNIT- IV:

Encryption Techniques: Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

Designing Secure Networks: Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, the Difficulties of Secure Networking, Security Technologies, Emerging Security Technologies General Design Considerations, Layer 2 Security Considerations, IP Addressing Design Considerations - ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

Text Books:

1. William Stallings, Cryptography and Network Security Principles And Practices, 3rd ed., Pearson Education, 2003.
2. Sean Convery, Network Security Architectures, 1st ed., Cisco Press, 2004.

Reference Books:

1. Atul Kahate, Cryptography and Network Security,2nd ed., Tata McGraw Hill, 2003.
2. Bruce Schneier, Applied Cryptography, 2nd ed., John Wiley and Sons Inc, 1996.

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M.Tech II Semester (VLSI)

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(13VL208) REAL TIME OPERATING SYSTEMS
(ELECTIVE-II)

UNIT- I:

Introduction to UNIX: Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

Real Time Systems: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

UNIT- II:

Approaches to Real Time Scheduling: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

Operating Systems: Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

UNIT- III:

Fault Tolerance Techniques: Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

Case Studies – VX Works: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

UNIT- IV:

RT Linux: Process Management, Scheduling, Interrupt Management, and Synchronization

Text Books:

1. Richard Stevens, Advanced Unix Programming, 2nd ed., Addison-Wesley, 2005.
2. Jane W.S. Liu, Real Time Systems, 1st ed., Pearson Education, 2000.
3. C.M.Krishna, KANG G. Shin, Real Time Systems, McGraw.Hill, 1997.

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M.Tech II Semester (VLSI)

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(13VL209) MIXED SIGNAL LAB

1. Analog Circuits Simulation using Spice.
2. Mixed Signal Simulation Using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
6. Net List Extraction.
7. Design Rule Checks.

NOTE: Required Software Tools:

1**.** Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)

2. Xilinx 9.1i and Above for FPGA/CPLDS.

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M.Tech II Semester (VLSI)	L	T	P	[C]
	0	0	3	[2]

(13VL210) EMBEDDED PROCESSING LAB

1. Study of different addressing modes Using 89C51/PIC microcontroller.

2. General purpose input output (GP10) ports using 89C51/PIC microcontroller

3. Keyboard Interface using embedded micro controller.

4. LED and LCD Interface using 89C51/PIC Micro controller.

5. RTD and Thermocouple Interface using embedded micro controller

6. ADC and DAC Interface using embedded micro controller.

7. I^2C RTC interface using embedded micro controller

8. Alarm clock using embedded micro controller.

9. Testing RTOS Environment and System Programming using KEIL software.

10. Flash controller programming - Data flash with erase , verify, fusing through ATMEL/INTEL tools.

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(13VL211) TERM PAPER

The Term Paper is a precursor to the project work done in the 2nd year M.Tech Programme. The paper may be of 8-10 (A4 size) in length and follows the standard IEEE/Technical Journal Format.

The Term Paper helps to supplement the second year Project Work of the M.Techstudents. It helps to identify their Reserch area/topic and complete the groundwork andpreliminary research required for it comfortably. It trains the students to make use of Research Tools and Material available both in print and digital formats.

Based on the topic, a hypothesis is to be made by the student, under the supervision of the guide. The student is then required to collect literature and support information for his / her term paper from Standard Reference Books, Journals, and Magazines - both printed and online. Each student should refer to a minimum of 6 reference sources related to the topic. The student also presents his/her paper with the help of Power Point slides / OHP.

The Term Paper contains: The Aim and Objective of the study, The need for Rationale behind the study, Identify the work already done in the field, Hypothesis and Discussion, Conclusion Appendix with support data (Illustrations, Tables, Graphs, etc.).

Page Limit: minimum of eight pages.

Date of evaluation: During the Lab Internal Exam.

Method of Evaluation**:** Total 50 marks

1. Day to day work - 10 marks
2. Term Paper Report - 20 marks
3. Seminar - 20 marks

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M.Tech III & IV Semesters (VLSI)	L	T	P	[C]
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(13VL401) SEMINAR-II

Objectives: To get involved with the latest advancements and developments to enhance communication and presentation skills, exchange of ideas, greater connectivity to develop a research bent of mind.

For the seminar, the student shall collect the information on a specialized relevant topic and prepare a report, showing his understanding over the topic, and submit the same to the department, which shall be evaluated by the Department Committee consisting of Head of the department, Seminar Supervisor and a Senior Faculty Member. Each Seminar shall be evaluated for 50 marks (10 marks for report, 10 marks for subject content, 20 marks for presentation and 10 marks for queries).

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M.Tech III & IV Semesters (VLSI)	L	T	P	[C]
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(13VL402) PROJECT WORK

Students are required to take up a project work, in which the student can choose any specific problem of Industry or Industry based project work. Alternatively it can be secondary source based or Field based project work. Before the commencement of the project work each student is required to submit a synopsis indicating the objectives, Methodology, Framework for analysis, Action plan with milestones in order to have clarity for the subsequent work. The project should have an internal faculty as guide. The student can initiate the project work in the penultimate semester of the course.