



AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

Gudur, Nellore Dist - 524101, A.P (India)

ACADEMIC REGULATIONS FOR THE AWARD OF FULL TIME M.Tech DEGREE PROGRAMME (WITH EFFECT FROM THE ACADEMIC YEAR 2013-14)

The **Audisankara College of Engineering and Technology**, Gudur, Nellore District, Andhra Pradesh shall confer M.Tech Post Graduate degree to candidates who are admitted to the Master of Technology Programs and fulfill all the requirements for the award of the degree.

1. ELIGIBILITY FOR ADMISSIONS:

Admission to the Master of Technology programme shall be made subject to the eligibility, qualifications and specialization criteria prescribed by the JNTUA, Anantapur for each programme, from time to time.

As per the norms of A.P. State Council of Higher Education (APSCHE), Government of Andhra Pradesh, admissions are made to the first year of two years M.Tech P.G. Degree Programme as follows:-

- As per the norms of Government of Andhra Pradesh, Category-A (based on the rank obtained in GATE / PGCET score) seats will be filled by the Convener, PGCET.
- As per the norms of Government of Andhra Pradesh, Category-B seats will be filled by the management.

2. COURSE WORK:-

- ❖ A Candidate after securing admission must pursue the M.Tech course of study for Four Semesters duration.
- ❖ Each semester shall be of 20 weeks duration including all examinations.
- ❖ A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

3.0 ATTENDANCE REGULATIONS AND CONDONATION:-

- (i) A student shall be eligible to appear for end semester examinations, if he acquires a minimum of 75% attendance in aggregate of all the subjects.
- (ii) Condonation of shortage of attendance in aggregate up to 10% on medical grounds (65% above and below 75%) in each semester may be granted on the recommendation of the College Academic Committee. However, granting condonation is purely at the discretion of Principal of the college.
- (iii) A Student will not be promoted to the next semester unless he satisfies the attendance requirement of the present semester as applicable. They may seek re-admission for that semester as and when offered next.
- (iv) Shortage of Attendance below 65% in aggregate shall in no case be condoned.
- (v) Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examinations of that particular semester and their registration for examination shall stand cancelled.

- (vi) A stipulated fee shall be payable towards condonation of shortage of attendance if granted.
- (vii) Attendance may also be condoned for those students who participate in prestigious sports and co and extracurricular activities provided their attendance is in the minimum prescribed range for the purpose and recommended by the concerned authority.

4.0. **EVALUATION:-**

The performance of the candidate in each semester shall be evaluated subject-wise for a maximum of 100 marks for Theory and 100 marks for practical subjects, on the basis of Internal Evaluation and End Semester Examination. For the theory & practical subjects 60% of the marks will be for the External End Examination, while 40% of the marks for Internal Evaluation.

4.1 INTERNAL EVALUATION FOR THEORY SUBJECTS:

Each course is evaluated for **40 marks (a+b)**

a) Two Midterm Examinations each for 30 marks with a duration of two hours each will be conducted for every theory course in a semester. First Midterm Examination is conducted in the middle of the Semester (I & II units) and second Midterm Examination immediately after the completion of instruction (III & IV units) as per academic schedule. The Midterm Examination marks shall be awarded giving a weightage of 80% in the Midterm Examination in which the student scores more marks and 20% in the remaining Midterm Examination.

Midterm Examination Pattern for 30 Marks:

- ❖ Each Midterm Examination Question Paper comprises of four questions covering the two units.
- ❖ Answering any three questions.
- ❖ Questions 1 & 2 from one unit and Questions 3 & 4 from another unit. Each question is allotted 10 marks.

b) 10 marks are allocated for **Assignment Tests**.

- ❖ There will be four Assignment Tests per subject.
- ❖ One Assignment Test is conducted from each unit.
- ❖ Five Assignment questions are given in advance from each unit out of which two questions given by the concerned teacher has to be answered during Assignment Test.
- ❖ Average of Assignment Tests marks is considered.

NOTE: A student who is absent for any Midterm Examination / Assignment Test, for any reason whatsoever, shall be deemed to have scored zero marks in that Midterm Examination/ Assignment Test and no make-up test shall be conducted.

4.2 INTERNAL EVALUATION FOR PRACTICAL SUBJECTS:

For Laboratory courses there shall be continuous evaluation during the semester for 40 internal marks. The break-up of internal marks to be awarded is as given below:

Table 1: Break-up of Internal Marks

S.No.	Criterion	Marks
1	Conduct of experiments, Observation & Results in regular class work(Day-to-Day Performance)	25
2	Viva – voce and Internal Examination	15

In any semester a minimum of 90% of the prescribed number of experiments/exercises specified in the syllabus for laboratory course shall be conducted. They shall complete these experiments/exercises in all respects and submit report and get it certified by the concerned internal lab teacher and the Head of the Department to become eligible to appear for the final end examination in the Laboratory Course.

4.3 INTERNAL EVALUATION FOR SEMINAR-I & SEMINAR-II:

There shall be two Seminars conducted in each discipline, Seminar-I in the M.Tech I Semester and the Seminar-II in M.Tech IV semester. The distribution of internal marks for seminar is given below:

Table 2: Distribution of Marks

S.No.	Criterion	Marks
1	Seminar Report & Subject content	20
2	Seminar presentation & Viva – Voce Exam	30

For the seminar, the student shall collect the information on a specialized relevant topic and prepare a report, showing his understanding over the topic, and submit the same to the department, which shall be evaluated by the Department Committee consisting of Head of the department, Seminar Supervisor and a Senior Faculty Member. Each Seminar shall be evaluated for 50 marks (10 marks for report, 10 marks for subject content, 20 marks for presentation and 10 marks for queries).

4.4 TERM PAPER:

The Term Paper is a precursor to the project work done in the 2nd year M.Tech Programme. The paper may be of 8-10 (A4 size) in length and follows the standard IEEE/Technical Journal Format.

The Term Paper helps to supplement the second year Project Work of the M.Tech students. It helps to identify their Research area/topic and complete the groundwork and preliminary research required for it comfortably. It trains the students to make use of Research Tools and Material available both in print and digital formats.

Based on the topic, a hypothesis is to be made by the student, under the supervision of the guide. The student is then required to collect literature and support information for his / her term paper from Standard Reference Books, Journals, and Magazines - both printed and online. Each student should refer to a minimum of 6 reference sources related to the topic. The student also presents his/her paper with the help of Power Point slides / OHP.

The Term Paper contains: The Aim and Objective of the study, The need for Rationale behind the study, Identify the work already done in the field, Hypothesis and Discussion, Conclusion Appendix with support data (Illustrations, Tables, Graphs, etc.).

Page Limit: minimum of eight pages.

Date of evaluation: During the Lab Internal Exam.

Method of Evaluation: Total 50 marks

1. Day to day work - 10 marks
2. Term Paper Report - 20 marks
3. Seminar - 20 marks

4.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

4.6 In case the candidate does not secure the minimum academic requirement in any subject(as specified in 4.4) he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the course when next offered or do any other specified subject as may be required.

5.0 SEMESTER END EXAMINATIONS:-

5.1 Theory Courses: 60 marks each

The Semester end examination in each theory subject shall be conducted for 3 hours duration at the end of the semester for 60 marks. The question paper for Semester pattern shall be designed as per the following:

Question paper contains

- A total of Eight questions.
- Answer one Question from each Unit
- The Eight questions are to be designed taking one question from each unit (Unit Wise Either or Type) of the four units.
- In each question, one, two or more bits can be set, totaling 15 Marks with appropriate distribution of marks.

A student has to secure not less than a minimum of 40% of marks (24 marks) exclusively at the end semester examinations in each of the theory subjects in which the candidate had appeared. However, the candidate shall have to secure a minimum of 50% of marks (50 marks) in both external and internal components put together to become eligible for passing in the subject.

5.2 Lab Courses (Practical / Workshop): 60 marks

Out of 60 marks **40** marks are allocated for experiment (procedure for conducting the experiment carries 10 marks & readings, calculation and result-30 marks) and **15** marks for viva-voce examination with **5** marks for the record.

Each Semester External Lab Examination shall be evaluated by an Internal Examiner along with an External Examiner. External Examiner is appointed by the Principal.

A candidate shall be declared to have passed in individual lab course if he secures a minimum of 50% aggregate marks (50 marks) (Internal & Semester External Examination marks put together), subject to a minimum of 40% marks (24 marks) in the semester external examination.

5.3 EVALUATION OF PROJECT WORK:-

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ concerned department.

- ❖ **Registration of Project work:** A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Semesters)
- ❖ An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor/ Guide and one Internal senior expert shall monitor the progress of the project work.
- ❖ The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest and one calendar year from the date of registration for the project work. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

- ❖ The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.
- ❖ A candidate shall be allowed to submit the thesis / dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva-voce examination of the project. The viva-voce examination may be conducted once in two months for all the candidates submitted during that period.
- ❖ Three copies of the Thesis / Dissertation certified in the prescribed form by the supervisor and HOD shall be submitted to the HOD.
- ❖ The semester end examination for project work done during III & IV Semesters, shall be conducted by a Project Review Committee (PRC). The evaluation of project work shall be conducted at the end of the IV Semester.
- ❖ The PRC comprises of an External examiner appointed by the Principal, Head of the Department and Project Guide/Supervisor to adjudicate the thesis / dissertation. The PRC shall jointly evaluate candidates work and award grades as given below

S.No	Description	Grade
1	Very Good	Grade A
2	Good	Grade B
3	Satisfactory	Grade C
4	Not satisfactory	Grade D

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the thesis.

6.0 **RE-REGISTRATION FOR IMPROVEMENT OF INTERNAL EVALUATION MARKS:**

Following are the conditions to avail the benefit of improvement of internal evaluation marks.

- ❖ The candidate should have completed the course work and obtained examinations results for I & II semesters.
- ❖ He should have passed all the subjects for which the internal evaluation marks secured are more than 50%.
- ❖ Out of the subjects the candidate has failed in the examination due to Internal evaluation marks secured being less than 50%, the candidate shall be given one more chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.
- ❖ The candidate has to re-register for the subjects so chosen and fulfill all the academic requirements.
- ❖ For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of **'The Principal, Audisankara College of Engineering & Technology'** payable at Gudur along with the requisition through the Controller of the Examinations of the college.
- ❖ In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

7.0 SEMESTER – WISE DISTRIBUTION OF CREDITS:**Table 3: Semester –wise Credits distribution**

SEMESTER	No. of Credits per semester Theory + Lab	Total credits
I Semester	24+06	30
II Semester	24+06	30
III & IV Semesters	0+18	18
TOTAL CREDITS	48+30	78

8.0 AWARD OF DEGREE AND CLASS:-

A candidate shall be eligible for the award of degree if he satisfies the minimum academic requirements in every subject, Seminar and secures 'satisfactory' or higher grade report on his thesis/dissertation and viva-voce. Based on overall percentage of marks obtained, the following class is awarded.

Table 4: Award of Division

Class Awarded	% of marks to be secured
First Class with Distinction	70% and above
First Class	Below 70% but not less than 60%
Second Class	Below 60% but not less than 50%

9.0 READMISSION CRITERIA:

A Candidate, who is detained in a semester due to lack of attendance, has to obtain written permission from the Principal for readmission into the same semester after duly fulfilling all the required norms stipulated by the college in addition to paying the required fee.

10. SUPPLEMENTARY EXAMINATIONS:

Apart from the regular End Examinations the institute may also schedule and conduct supplementary examinations for all subjects for the benefit of students with backlogs. Such students writing supplementary examinations as supplementary candidates may have to write more than one examination per day.

11. CONDUCT AND DISCIPLINE:-

- (a) Students shall conduct themselves within and outside the premises of the Institute in a descent and dignified manner befitting the students of ACET.
- (b) As per the order of the Honorable Supreme Court of India, ragging in any form is considered a criminal offence and is totally banned. Any form of ragging will be severely dealt with.
- (c) The following acts of omission and / or commission shall constitute gross violation of the code of conduct and are liable to invoke disciplinary measures with regard to ragging.
 - (i) Lack of courtesy and decorum; indecent behavior anywhere within or outside the college campus.
 - (ii) Damage of college property or distribution of alcoholic drinks or any kind of narcotics to fellow students / citizens.
- (d) Possession, consumption or distribution of alcoholic drinks or any kind of narcotics or hallucinogenic drugs.
- (e) Mutilation or unauthorized possession of library books.

- (f) Noisy and unruly behavior, disturbing studies of fellow students.
- (g) Hacking in computer systems (such as entering into other person's areas without prior permission, manipulation and / or damage of computer hardware and software or any other cyber crime etc.
- (h) Usage of camera /cell phones in the campus.
- (i) Plagiarism of any nature.
- (j) Any other act of gross indiscipline as decided by the college academic council from time to time.
- (k) Commensurate with the gravity of offense, the punishment may be reprimand, fine, expulsion from the institute/ hostel, debarring from examination, disallowing the use of certain facilities of the Institute, rustication for a specified period or even outright expulsion from the Institute, or even handing over the case to appropriate law enforcement authorities or the judiciary, as required by the circumstances.
- (l) For an offence committed in (i) a hostel (ii) a department or in a class room and (iii) elsewhere, the chief Warden, the concern Head of the Department and the Principal respectively, shall have the authority to reprimand or impose fine.
- (m) Cases of adoption of unfair means and/ or any malpractice in an examination shall be reported to the principal for taking appropriate corrective action.
- (n) All cases of serious offence, possibly requiring punishment other than reprimand, shall be reported to the Academic council of the college.
- (o) The Institute Level Standing Disciplinary Action Committee constituted by the academic council shall be the authority to investigate the details of the offence, and recommend disciplinary action based on the nature and extent of the offence committed.
- (p) The Principal shall deal with any problem, which is not covered under these rules and regulations.
- (q) **"Grievance and Redressal Committee" (General)** constituted by the Principal shall deal with all grievances pertaining to the academic / administrative / disciplinary matters.
- (r) All the students must abide by the code and conduct rules prescribed by the college from time to time.

12.0 WITH – HOLDING OF RESULTS:

If the candidate has not paid dues to the university/college or if any case of in-discipline is pending against him, the result of the candidate shall be withheld and he will not be allowed / promoted to the next higher semester. The issuing of degree is liable to be withheld in such cases.

13.0 TRANSITORY REGULATIONS:

Candidates who have discontinued or have been detained for want of attendance or who have failed after having undergone the course in earlier regulations and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when such subjects are offered, subject to the conditions of 4.5 and 2.3 sections.

14.0 MINIMUM INSTRUCTION DAYS:

The minimum instruction days for each semester shall be 90 clear instruction days excluding the days allotted for tests/examinations and preparation holidays declared if any.

15.0AMENDMENTS OF REGULATIONS-

The college may, from time to time, revise, amend or change the regulations, scheme of examinations and syllabi. However the academic regulations of any student will be same throughout the course of study in which the student has been admitted.

16.0 GENERAL:

- ❖ The academic regulations should be read as a whole for the purpose of any interpretation.
- ❖ Disciplinary action for Malpractice/improper conduct in examinations is appended.
- ❖ Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.
- ❖ In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Head of the Institute is final.

RULES FOR DISCIPLINARY ACTION FOR MALPRACTICE / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	<i>If the candidate</i>	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Is found copying in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate will be cancelled.
3.	Comes in alcohol drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
4.	Smuggles the Answer book or a part there of additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of

		seat.
5.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
6.	Possesses any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate will also be debarred and forfeit the seat.
7.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate will also be debarred and forfeit the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate will also be debarred for two consecutive semesters from class work and all end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case registered against him.
8.	Refuses to obey the orders of the Chief Superintendent/Asst.Superintendent/ any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall causing any injury to him or to any of his relations	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are

	whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case registered against them.
9.	Is a student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clauses 6 to 8.	In case of students of the college expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
11.	Is detected copying on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	Indulging in any malpractice which is not covered in the above clauses 1 to 11 if detected shall be reported to the College Authorities for further action to award suitable punishment.	Appropriate action will be taken as recommended by the College Authorities.

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.



**AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)**

Gudur, Nellore Dist - 524101, A.P (India)

Course Structure for M.Tech (ES) Regular Programme
Applicable for students admitted from Academic Year 2013-14

M.Tech I Year (I Semester) - Embedded Systems

Sl.No	Course Code	Subject	Scheme of instruction (Periods / week)		Scheme of Examination			No. of Credits
			Theory	Lab	IM	EM	Total Marks	
1	13ES101	Micro Controllers and Interfacing	4	-	40	60	100	4
2	13ES102	Operating Systems	4	-	40	60	100	4
3	13ES103	Embedded System Concepts	4	-	40	60	100	4
4	13ES104	VLSI Technology and Design	4	-	40	60	100	4
5	13ES105	DSP Processors and Architectures	4	-	40	60	100	4
6	13ES106	<u>Elective-I</u>	4		40	60	100	4
	13ES107	1.Digital IC Design						
	13ES108	2.Advanced Computer Architecture						
7	13ES109	3.Algorithms for VLSI Design Automation						
7	13ES109	Microcontrollers and Interfacing Lab	-	3	40	60	100	2
8	13ES110	IC System Design Lab	-	3	40	60	100	2
9	13ES111	Seminar-I	-	-	50	-	50	2
Contact Periods / Week			24	6	370	480	850	30
			Total Periods/ Week		30	Total Credits		

M.Tech I Year (II Semester) - Embedded Systems

Sl.No	Course Code	Subject	Scheme of instruction (Periods / week)		Scheme of Examination			No. of Credits
			Theory	Lab	IM	EM	Total Marks	
1	13ES201	FPGA Architecture and Applications	4	-	40	60	100	4
2	13ES202	Real Time Operating Systems	4	-	40	60	100	4
3	13ES203	System on Chip (SOC)	4	-	40	60	100	4
4	13ES204	Cryptography and Network Security	4	-	40	60	100	4
5	13ES205	Hardware Software Co-Design	4	-	40	60	100	4
6	13ES206 13ES207 13ES208	Elective-II 1. Robotic Technology 2. Microelectromechanical Systems (MEMS) 3. Software Defined Radio	4		40	60	100	4
7	13ES209	RTOS and FPGA Lab	-	3	40	60	100	2
8	13ES210	Advanced Embedded Systems Lab	-	3	40	60	100	2
9	13ES211	Term Paper	-	-	50	-	-	2
Contact Periods / Week			24	3	370	480	850	30
			Total Periods/ Week		27	Total Credits		

M.Tech II Year (III & IV Semesters) - Embedded Systems

Sl.No	Course Code	Subject	Scheme of Examination			No. of Credits
			IM	EM	Total Marks	
1	13ES401	Seminar-II	50	-	50	2
2	13ES402	Project Work	-	A/B/C/D		16
Contact Periods / Week						18
			Total Credits			

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

Detailed Syllabus

M.Tech I Semester (ES)

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(13ES101) MICROCONTROLLERS AND INTERFACING

UNIT- I:

Intel 8051: Architecture of 8051, Memory Organization, Register banks, Bit addressing media, SFR area, addressing modes, Instruction set, Programming examples. 8051 Interrupt structure, Timer modules, Serial Features, Port structure, Power saving modes.

UNIT- II:

Motorola HC11: Controllers features, Different modes of operation and memory map, Functions of I/O ports in single chip and expanded multiplexed mode, Timer system. Input capture, Output compare and pulsed accumulator features of 68HC11, Serial peripherals, Serial Communication interface, Analog to digital conversion features.

UNIT- III:

Pic Microcontrollers: Program memory, CPU registers, Register file structure, Block diagram of PIC 16C74, I/O ports. Timer 0,1 and 2 features, Interrupt logic, serial peripheral interface, I²C bus, ADC, UART, PIC family parts.

Microcontrollers Interfacing: 8051, 68HC11, PIC-16C6X and ATMEL External Memory Interfacing – Memory Management Unit, Instruction and data cache, memory controller. On Chip Counters, Timers, Serial I/O, Interrupts and their use. PWM, Watch dog, ISP, IAP features.

UNIT- IV:

Interrupt Synchronization: Interrupt vectors & priority, external interrupt design. Serial I/O Devices RS232 Specifications, RS422/Apple Talk/ RS 423/RS435 & other communication protocols. Serial Communication Controller.

Case Studies: Design of Embedded Systems using the micro controller 8051/ARM6TDMI, for applications in the area of Communications, Automotives, industrial control.

Text Books:

- 1.M.A. Mazadi,J.G. Mazidi,The 8051 Micro Controller &Embedded Systems, Pearson Education,2000.
- 2.John B. Peatman, Designing with PIC Micro Controllers,1st ed., Pearson Education,1997.
- 3.Jonathan W. Valvano, Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning, 1999.

Reference Books:

- 1.8-bit Embedded Controllers, INTEL Corporation 1990.
- 2.John B.Peatman, Designing with PIC Microcontrollers, Pearson Education Inc, India, 2005.

AUDISANKARA COLLEGE OF ENGINEERING & TECHNOLOGY: GUDUR (AUTONOMOUS)

M.Tech I Semester (ES)

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(13ES102) OPERATING SYSTEMS

UNIT- I:

Introduction: Operating system definition, Objective and functions, types, different parts, Structure of operating system, trends- parallel computing, distributed computing; Open systems, Hardware, software, firmware

Process Scheduling: Definition of a process; process states, transitions, process control, suspend and process, interrupt processing, nucleus of an operating system; parallel processing; Mutual exclusion, Critical Section; Solution of mutual exclusion; Semaphores; Deadlock- occurrence, prevention, detection and recovery;

UNIT- II:

Storage Management: Storage organization, management strategies, hierarchy; virtual storage, paging, segmentation.

File System Management: File system (function of a file system)- data hierarchy, blocking and buffering, file organization, queued and basic access methods, backup and recovery;

UNIT –III:

I/O Management: (functions of I/O management subsystem), Distributed computing- OSI view, OSI network management, MAP, TOP, GOSIP, TCP/IP;

OS Security: Requirements, external security, operational security, surveillance, threat monitoring; Introduction to Cryptography.

UNIT- IV:

Case Studies: UNIX- Shell, Kernel, File System, Process Management, Memory Management, I/O System, Distributed UNIX; Example of operating system-MS-DOS, Windows, OS/2, Apple Macintosh & Linux.

Text Books:

1. Dietal H.M , *An Introduction to OS*, 12th Indian Reprint , PHI New Delhi, 2003.
2. Andrew S.Tanenbaum, *Modern OS*, 3rd Indian Reprint, PHI Pearson Education, 2004.
3. Silberschatz . A, Galvin.p and Gagne.G, *Operating System Concepts*, John Wiley and Sons, 2002.

Reference Books:

1. William Stallings, *Operating Systems*, 7TH ed.,Pearson Education, 2011.
2. D.M. Dhamdhere, *Operating Systems – A Concept Approach*, 1st ed.,Tata McGraw Hill, 2003.

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M.Tech I Semester (ES)

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(13ES103) EMBEDDED SYSTEM CONCEPTS

UNIT- I:

Introduction to Embedded Systems: An Embedded System, Processor in The System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System -On-Chip (SOC) and in VLSI Circuit.

Processor and Memory Organization: Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

UNIT- II:

Devices and Buses for Device Networks: I/O Devices, Timer and Counting Devices, Serial Communication Using The "I²C" , CAN, Profibus Foundation Field Bus. and Advanced I/O Buses Between the Network Multiple Devices, Host Systems or Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses.

Device Drivers and Interrupts Servicing Mechanism: Device Drivers, Parallel Port and Serial Port Device Drivers in a System, Device Drivers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

UNIT- III:

Instruction Sets: Introduction, preliminaries, ARM processor, SHARC processor.

Programming Concepts and Embedded Programming in C, C++, VC++ and JAVA: Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

UNIT- IV:

Hardware- Software CO- Design in an Embedded System: Embedded System Project Management, Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, use of Target Systems, use of Software Tools for Development of an Embedded System, use of Scopes and Logic Analysis for System, Hardware Tests. Issues in Embedded System Design.

Text Books:

1. Rajkamal, Embedded systems: Architecture, Programming and Design, TMH, 2008.
2. wayne wolf, Computers as a component: principles of embedded computing system design.

Reference Books:

1. Arnold S Berger, Embedded System Design, 1st ed., CMP Books, 2001.
2. An embedded software primer by David Simon, 1st Indian Reprint, PEA, 2001.
3. Steve Heath, Embedded systems design: Real world design , Newton Mass USA, 2002.
4. Hayt, Data communication.

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(13ES104) VLSI TECHNOLOGY AND DESIGN

UNIT- I:

Review of Microelectronics and Introduction to MOS Technologies: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

Basic Electrical Properties of MOS, CMOS & BICOMS Circuits: I_{ds} - V_{ds} Relationships, Threshold Voltage V_t , G_m , G_{ds} and W_o , Pass Transistor, MOS, CMOS & Bi- CMOS Inverters, Z_{pu}/Z_{pd} , MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT- II:

Layout Design and Tools: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT- III:

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

Sequential Systems: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT- IV:

Floor Planning & Architecture Design: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOC's and Embedded CPUs, Architecture Testing.

Introduction to CAD Systems (Algorithms) and Chip Design: Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

Text Books:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian et . al(3 authors), PHI of India Ltd.,2005
2. Wayne Wolf, Modern VLSI Design, 3rd ed., Pearson Education,2005.

Reference Books:

1. N.H.E Weste, K.Eshraghian, Addison Wesley, Principles of CMOS Design, 2nd ed.,1993.
2. Fabricius, Introduction to VLSI Design, MGH International Edition, 1990.
3. Baker, Li Boyce, CMOS Circuit Design, Layout and Simulation, PHI, 2004.

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(13ES105) DSP PROCESSORS AND ARCHITECTURES

UNIT- I:

Introduction to Digital Signal Processing Introduction, Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

Computational Accuracy in DSP Implementations

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT- II:

Architectures for Programmable DSP Devices

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Execution Control and Pipelining

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT- III:

Programmable Digital Signal Processors

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

Implementations of Basic DSP Algorithms

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT- IV:

Implementation of FFT Algorithms

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

Interfacing Memory and I/O Peripherals to Programmable DSP Devices

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

Text Books:

1. Avtar Singh and S. Srinivasan, Digital Signal Processing, Thomson Publications, 2004.
2. Lapsleyetal, DSP Processor Fundamentals, Architectures & Features, S.Chand & Co, 2000.

Reference Books:

1. B. Venkata Ramani, M. Bhaskar, Digital Signal Processors, Architecture, Programming and Applications, 4th ed. Reprint,TMH,2008.
2. Jonatha Stein, Digital Signal Processing ,1st ed., John Wiley, 2005.

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**(13ES106) DIGITAL IC DESIGN
(ELECTIVE-I)**

UNIT- I:

CMOS inverters -static and dynamic characteristics.

Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

UNIT- II:

Method of Logical Effort for Transistor Sizing -power consumption in CMOS gates- Low power CMOS design.

Arithmetic Circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

UNIT- III:

Bipolar gate Design- BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.

Layout Design Rules: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load.

UNIT- IV:

Subsystem Design Process: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

Text Books:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, 2nd ed., MGH, 1999.
2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, 2nd ed., Prentice Hall, 2003.
3. Eugene D Fabricus, Introduction to VLSI Design, McGraw Hill International Edition, 1990.

REFERENCES:

1. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000.
2. Neil H E West and Kamran Eshraghian, Principles of CMOS VLSI Design: A System Perspective", 2nd ed., Addison-Wesley, 2002.
3. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, 3rd ed., McGraw-Hill, 2004.

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**(13ES107) ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE-I)**

UNIT- I:

Fundamentals of Computer Design: Technology trends, cost- measuring and reporting performance quantitative principles of computer design.

Instruction Set Principles and Examples: Classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set- instructions for control flow- encoding an instruction set.-the role of compiler

UNIT- II:

Instruction Level Parallelism (ILP): Over coming data hazards, reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP

ILP Software Approach: Compiler Techniques, Static Branch Protection, VLIW Approach, H.W support for more ILP at compile time- H.W verses S.W solutions

UNIT- III:

Memory Hierarchy Design: Cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

Multiprocessors and Thread Level Parallelism: Symmetric shared memory architectures, distributed shared memory, Synchronization, multi threading.

UNIT- IV:

Storage Systems: Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

Inter Connection Networks and Clusters: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster

Text Books:

1. John. Hennessy & David A. Patterson Morgan Kufmann, *Computer Architecture- A quantitative approach*, 5th ed., Elsevier, 2011.

Reference Books:

1. Kai Hwang and A. Briggs, *Computer Architecture and parallel Processing*, International Edition McGraw-Hill, 1984.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, *Advanced Computer Architectures*, Pearson.

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**(13ES108) ALGORITHMS FOR VLSI DESIGN AUTOMATION
(ELECTIVE-I)**

UNIT- I:

Preliminaries: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

General Purpose Methods for Combinational Optimization: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT- II:

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

Modelling and Simulation: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT- III:

Logic Synthesis and Verification: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

High – Level Synthesis: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT- IV:

Physical Design Automation of FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

Physical Design Automation of MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

Text Books:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", Wiley Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd edition, Springer International Edition, 2005.

Reference Books:

1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", Wiley, 1993.
2. Wayne Wolf, "Modern VLSI Design: Systems on silicon", 2nd ed., Pearson Education Asia, 1998.

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M.Tech I Semester (ES)

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(13ES109) MICROCONTROLLERS AND INTERFACING LAB

Assembly:

1. Write a program to a) Clear the Register and b) Add 3 to Register Ten Times and Place the Result into Memory Use the Indirect Instructions to Perform Looping.

Programming in C:

2. A Door Sensor is connected to RB1 Pin and a Buzzer is connected to RB7. Write a Program to monitor Door Sensor and when it Open, Sounds the Buzzer by sending a Square Wave of few Hundred Hz Frequency to it.
3. Write a Program to Toggle all the Bits of PORT B parts continuously with a 250ns Delay.
4. Stepper Motor Control using Microcontroller.

Use Microcontrollers for the following Experiments.

Interfacing:

5. Elevator Interface.
6. Key Board Interface.
7. LED Interface.
8. Temperature Sensor.
9. SORT RTO'S on to 89c51 Board.
10. Sample the Signal using ADC and Reconstruct by using DAC.

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(13ES110) I C SYSTEM DESIGN LAB

List of the Experiments:

1. Design and Simulation of Arithmetic /logic operator circuits using verilog/VHDL
2. Modeling of Combinational/Sequential Circuits Using Verilog HDL
3. Simulation of schematic /RTL using Xilinx ISE Tool
4. ARBITER Design using state diagram in Xilinx ISE Tool
5. Simulation of HDL Netlist using Test bench
6. Modeling of MAC unit using verilog / VHDL
7. Modeling of ALU using verilog / VHDL
8. Design and 8-bit signed multiplication algorithm using verilog / VHDL
9. Design and technological mapping of RTL netlist in Xilinx ISE tool

NOTE: Required Software Tools:

1. Mentor Graphic tools / Cadance tools/ Synophysis tools. (180 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

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(13ES111) SEMINAR-I

Objectives: To get involved with the latest advancements and developments to enhance communication and presentation skills, exchange of ideas, greater connectivity to develop a research bent of mind.

For the seminar, the student shall collect the information on a specialized relevant topic and prepare a report, showing his understanding over the topic, and submit the same to the department, which shall be evaluated by the Department Committee consisting of Head of the department, Seminar Supervisor and a Senior Faculty Member. Each Seminar shall be evaluated for 50 marks (10 marks for report, 10 marks for subject content, 20 marks for presentation and 10 marks for queries).

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(13ES201) FPGA ARCHITECTURE AND APPLICATIONS

UNIT- I:

Programmable Logic: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypress FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

FPGA: Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

UNIT- II:

Case Studies: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

Finite State Machines(FSM): Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

UNIT- III:

Realization of State Machine: Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

FSM Architectures and Systems Level Design: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

UNIT- IV:

Digital Front End Digital Design Tools for FPGAS & ASICS: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

Text Books:

1. P.K.Chan & S. Mourad, *Digital Design Using Field Programmable Gate Array*, Prentice Hall, 1994.
2. S.Trimberger, Edr., *Field Programmable Gate Array Technology*, Kluwer Academic Publications, 1994.

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(13ES202) REAL TIME OPERATING SYSTEMS

UNIT- I:

Introduction to UNIX: Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

Real Time Systems: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

UNIT- II:

Approaches to Real Time Scheduling: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

Operating Systems: Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

UNIT- III:

Fault Tolerance Techniques: Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

Case Studies – VX Works: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

UNIT- IV:

RT Linux: Process Management, Scheduling, Interrupt Management, and Synchronization

Text Books:

1. Richard Stevens, *Advanced Unix Programming*,
2. Jane W.S. Liu, *Real Time Systems*, Pearson Education.
3. C.M.Krishna, KANG G. Shin, *Real Time Systems*, McGraw.Hill

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(13ES203) SYSTEM ON CHIP (SOC)

UNIT- I:

System on Chip Technology Challenges, System On a Chip (SOC) components, SOC Design Methodology, Parameterized Systems-on-a-Chip.

UNIT- II:

System-on-a-chip Peripheral Cores, SOC and interconnect centric Architectures, System level design representations and modeling languages.

UNIT- III:

Target architecture models, Intra-chip communication Graph partitioning algorithm, Task time measurement, Interconnect latency modeling.

UNIT- IV:

Back annotation of lower level timing to high-level models, Synthesis of SOC components, System Level, Block Level and Hardware/Software Co-verification,
SOC components: emulation, co-simulation, Physical Verification

Text Books:

- 1) Wayne Wolf, Modern VLSI Design: SOC Design, 3rd ed., Pearson Education, 2005.
- 2) Prakash Rashnikar, Peter Paterson, Lenna Singh, System-On-A-Chip Verification methodology & Techniques, Kluwer Academic Publishers.
- 3) Alberto Sangiovanni Vincentelli, Surviving the SOC Revolution: A Guide to Platform based Design", Kluwer Academic Publishers

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(13ES204) CRYPTOGRAPHY AND NETWORK SECURITY

UNIT- I:

Symmetric Ciphers: Overview – classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

Public – Key Encryption and Hash Functions: Introduction to Number Theory, Public-Key Cryptography and RSA, Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

UNIT- II:

Network Security Practice: Authentication Applications, Kerberos, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

System Security: Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

UNIT- III:

Wireless Security: Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

Secure Networking Threats: Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

UNIT- IV:

Encryption Techniques: Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

Designing Secure Networks: Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, the Difficulties of Secure Networking, Security Technologies, Emerging Security Technologies General Design Considerations, Layer 2 Security Considerations, IP Addressing Design Considerations - ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

Text Books:

1. William Stallings, Cryptography and Network Security Principles And Practices, 3rd ed., Pearson Education, 2003.
2. Sean Convery, Network Security Architectures, 1st ed., Cisco Press, 2004.

Reference Books:

1. Atul Kahate, Cryptography and Network Security, 2nd ed., Tata McGraw Hill, 2003.
2. Bruce Schneier, Applied Cryptography, 2nd ed., John Wiley and Sons Inc, 1996.

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(13ES205) HARDWARE SOFTWARE CO-DESIGN

UNIT- I:

Co-Design Issues: Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware- software partitioning distributed system co-synthesis.

UNIT- II:

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT- III:

Compilation Techniques and Tools for Embedded Processor:

Architectures: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT- IV:

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

Text Books:

1. Jorgen Staunstrup, Wayne Wolf, *Hardware / software co- design Principles and Practice*, Springer, 2009.
2. *Hardware / software co- design Principles and Practice*, 2002, Kluwer Academic Publishers

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(13ES206) ROBOTIC TECHNOLOGY (ELECTIVE-II)

UNIT-I:

Robot Fundamentals: Definitions, History of robots, present and future trends in robotics, Robot classifications, Robot configurations, Point to Point robots, Continuous Path robots, Work volume, Issues in design and controlling robots Repeatability, Control resolution, spatial resolution, Precision, Accuracy, Robot configurations, Point to Point robots, Continuous Path robots, Work volume, Applications of robots. Drives used in robots- Hydraulic, Pneumatic and Electric drives, Comparison of drive systems and their relative merits and demerits.

UNIT-II:

Manipulator Kinematics: Matrix Algebra, Inverse of matrices, rotational groups, matrix representations of coordinate transformation, transformation about reference frame and moving frame Forward & Inverse Kinematics examples of 2R, 3R & 3P manipulators, Specifying position and orientation of rigid bodies Euler's angle and fixed rotation for specifying position and orientation Homogeneous coordinate transformation and examples D-H representation of kinematics linkages Forward kinematics of 6R manipulators using D-H representations Inverse kinematics of 6R manipulators using D-H representations, Inverse Kinematics geometric and algebraic methods.

Unit- III:

Robotics Dynamics: Velocity Kinematics, Acceleration of rigid body, mass distribution Newton's equation, Euler's equation, Iterative Newton –Euler's dynamic formulation, closed dynamic, Lagrangian formulation of manipulator dynamics, dynamic simulation, computational consideration.

Trajectory Planning: Introduction, general considerations in path description and generation, joint space schemes, Cartesian, space schemes, path generation in runtime, planning path using dynamic model point to point and continuous trajectory, 4-3-4 & trapezoidal velocity strategy for robots.

UNIT-IV:

Robot Sensors: Internal and external sensors, position- potentiometric, optical sensors ,encoders - absolute, incremental, touch and slip sensors velocity and acceleration sensors, proximity sensors, force & torque sensors, laser range finder, camera. Micro-controllers, DSP, centralized controllers, real time operating systems.

Robot Controllers: Essential components-Drive for Hydraulic and Pneumatic actuators, H-bridge drives for Dc motor, Overload over current and stall detection methods, example of a micro-controller/ microprocessor based robot Controller.

Robot Vision: Introduction, Image acquisition, Illumination Techniques, Image conversion, Cameras, sensors, Camera and system interface, Frame buffers and Grabbers, Image processing, low level & high level machine vision systems.

Futuristic topics in Robotics: Micro-robotics and MEMS (Microelectro mechanical systems), fabrication technology for Micro-robotics, stability issue in legged robots, under-actuated manipulators.

Text Books:

- 1) S.R.Deb, *Robotics Technology and Flexible Automation* , Tata Mc Graw Hill 1994.
- 2) M.P.Groover, M. Weiss R.N. Nagel, N.G. Odrey, *Industrial Robotics (Technology, Programming and applications)* , McGraw, Hill 1996.
- 3) K.S.Fu, R.C.Gonzalez and C.S.G.Lee, *Robotics : Control , sensors , vision and intelligence* McGraw- Hill, 1987.
- 4) J.J.Craig , *Introduction to Robotics* , Addison-wesely 1989.

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**(13ES207) MICROELECTROMECHANICAL SYSTEMS (MEMS)
(ELECTIVE-II)**

UNIT- I:

Introduction, Basic Structures of MEM Devices: (Canti Levers, Fixed Beams diaphragms). Broad Response of Micro Electromechanical Systems (MEMs) to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic stimuli, Compatability of MEMS from the point of Power Dissipation, Leakage etc.

UNIT- II:

Review of Mechanical Concepts: Stress, Strain, Bending Moment, Deflection Curve. Differential Equations Describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed Beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with Voltage in C.L, Deflection Vs Voltage Curve, Critical Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions – Transient Response of the MEMS.

Two Terminal MEMS: Capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures. Three Terminal MEM Structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications.

UNIT- III:

MEM Circuits & Structures for Simple Gates: AND, OR, NAND, NOR, Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converters. Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature. Optical MEMS.

UNIT- IV:

MEM Technologies: Silicon Based MEMS – Process Flow – Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers Etc., Etching Technologies. Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes. Status of MEMS in the Current Electronics scenario.

Text Books:

1. Gabriel.M.Review, R.F. MEMS Theory, Design and Technology, John Wiley & Sons, 2003.
2. Thimo Shenko, *Strength of Materials*, CBS Publishers & Distributors., 2000.
3. Ristic L. (Ed.), *Sensor Technology and Devices*, Artech House, London 1994.
4. Servey E.Lyshevski, *MEMS and NEMS, Systems Devices and Structures*, CRC Press, 2002.

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**(13ES208) SOFTWARE DEFINED RADIO
(ELECTIVE-II)**

UNIT- I:

Software radio concepts, design principles, receiver front end topologies, noise and distortion in RF chain, digital generation of signals, common ADC and DAC architectures.

UNIT- II:

Object oriented software radios, Transmitter configuration, Digital compensation for analog I/O modulator errors, direct digital synthesizers, recursive oscillator.

UNIT- III:

CORDIC algorithm, pulse shaping and interpolation filters, resampling, DDS with tunable DSM, digital quad modulator, transmitter and receiver architectures.

UNIT- IV:

Power amplifier, switches, components, technology and modeling, case studies in software radio design.

Text Books::

1. Jouko Vanakka, *Digital Synthesizers and Transmitter for Software Radio*, Springer, 2005
2. A.A. Abidi et al, *ICs for Wireless Applications*, IEEE Press, 1999.

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(13ES209) RTOS AND FPGA LAB

List of Experiments:

1. RTOS System solution & tools
2. Testing RTOS Environment and System Programming.
 - a) Keil Tools
 - b) RTOS System Solutions with Tornado tools.
3. Embedded DSP based System Designing.
 - a) Code compressor studio (CCS) for embedded DSP using Texas tool kit.
 - b) Analog DSP tool kit.
4. Synthesis of the designs made using “VHDL / VERILOG and Mixed Design (VHDL & Verilog)” after Simulation is to be verified using FPGA/CPLD blocks from different commercially available Products on:
 - a) Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)
 - b) Synthesis of Sequential Circuits – 6 to 8 MSI and 1 or 2 VLSI Circuits.

NOTE: Required Software Tools for FPGA:

1. Mentor Graphic tools / Cadance tools/ Synophysis tools. (180 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

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(13ES210) ADVANCED EMBEDDED SYSTEMS LAB

List of Experiments:

1. PIC Programming and Interfacing.

- a) Program for addition of BCD numbers.
- b) Interface an LED array and 7-segment display
- c) Interfacing of PIC with LCD
- d) Interfacing of PIC with Keyboard Interfacing
- e) Interfacing of PIC with ADC, DAC
- f) Interfacing of PIC with temperature Sensor
- g) Interfacing of PIC with RTC
- h) Interfacing of PIC with DC Motor Control
- i) Interfacing of PIC with Stepper Motors

2. ARM Programming and Interfacing.

- (a) Introduction to ARM Development Tools.
- (b) Simple ARM Assembly Language and C Programming using ARM Kits.
- (c) LCD Interfacing.
- (d) Timer and Counter Programming.
- (e) Interfacing with Data Converters.
- (f) Serial Port Programming.
- (g) Interfacing with Sensors & Motors.
- (h) Generation of PWM.

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(13ES211) TERM PAPER

The Term Paper is a precursor to the project work done in the 2nd year M.Tech Programme. The paper may be of 8-10 (A4 size) in length and follows the standard IEEE/Technical Journal Format.

The Term Paper helps to supplement the second year Project Work of the M.Tech students. It helps to identify their Research area/topic and complete the groundwork and preliminary research required for it comfortably. It trains the students to make use of Research Tools and Material available both in print and digital formats.

Based on the topic, a hypothesis is to be made by the student, under the supervision of the guide. The student is then required to collect literature and support information for his / her term paper from Standard Reference Books, Journals, and Magazines - both printed and online. Each student should refer to a minimum of 6 reference sources related to the topic. The student also presents his/her paper with the help of Power Point slides / OHP.

The Term Paper contains: The Aim and Objective of the study, The need for Rationale behind the study, Identify the work already done in the field, Hypothesis and Discussion, Conclusion Appendix with support data (Illustrations, Tables, Graphs, etc.).

Page Limit: minimum of eight pages.

Date of evaluation: During the Lab Internal Exam.

Method of Evaluation: Total 50 marks

1. Day to day work - 10 marks
2. Term Paper Report - 20 marks
3. Seminar - 20 marks

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M.Tech III & IV Semesters (ES)

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(13ES401) SEMINAR-II

Objectives: To get involved with the latest advancements and developments to enhance communication and presentation skills, exchange of ideas, greater connectivity to develop a research bent of mind.

For the seminar, the student shall collect the information on a specialized relevant topic and prepare a report, showing his understanding over the topic, and submit the same to the department, which shall be evaluated by the Department Committee consisting of Head of the department, Seminar Supervisor and a Senior Faculty Member. Each Seminar shall be evaluated for 50 marks (10 marks for report, 10 marks for subject content, 20 marks for presentation and 10 marks for queries).

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(13ES402) PROJECT WORK

Students are required to take up a project work, in which the student can choose any specific problem of Industry or Industry based project work. Alternatively it can be secondary source based or Field based project work. Before the commencement of the project work each student is required to submit a synopsis indicating the objectives, Methodology, Framework for analysis, Action plan with milestones in order to have clarity for the subsequent work. The project should have an internal faculty as guide. The student can initiate the project work in the penultimate semester of the course.